Semiconductor Device Physics and Technology

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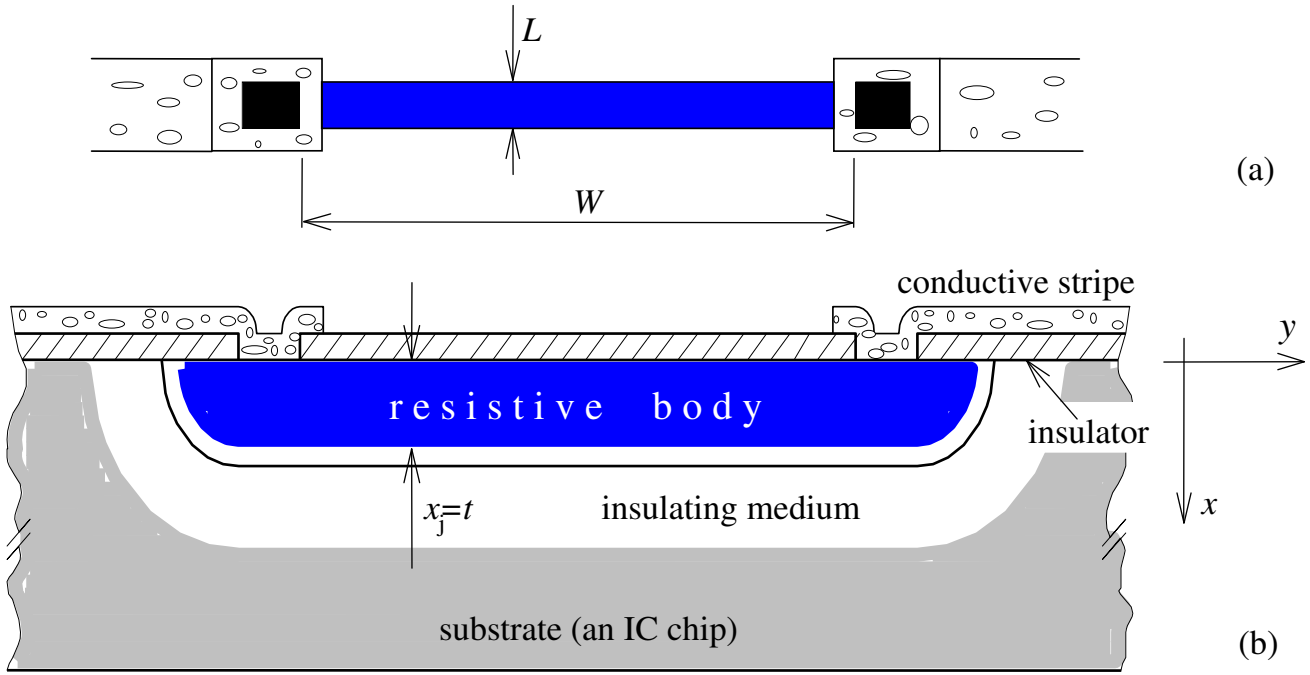
International Organization for Migration (IOM)
Organisation internationale pour les migrations (OIM)
Organización Internacional para las Migraciones (OIM)

Topics

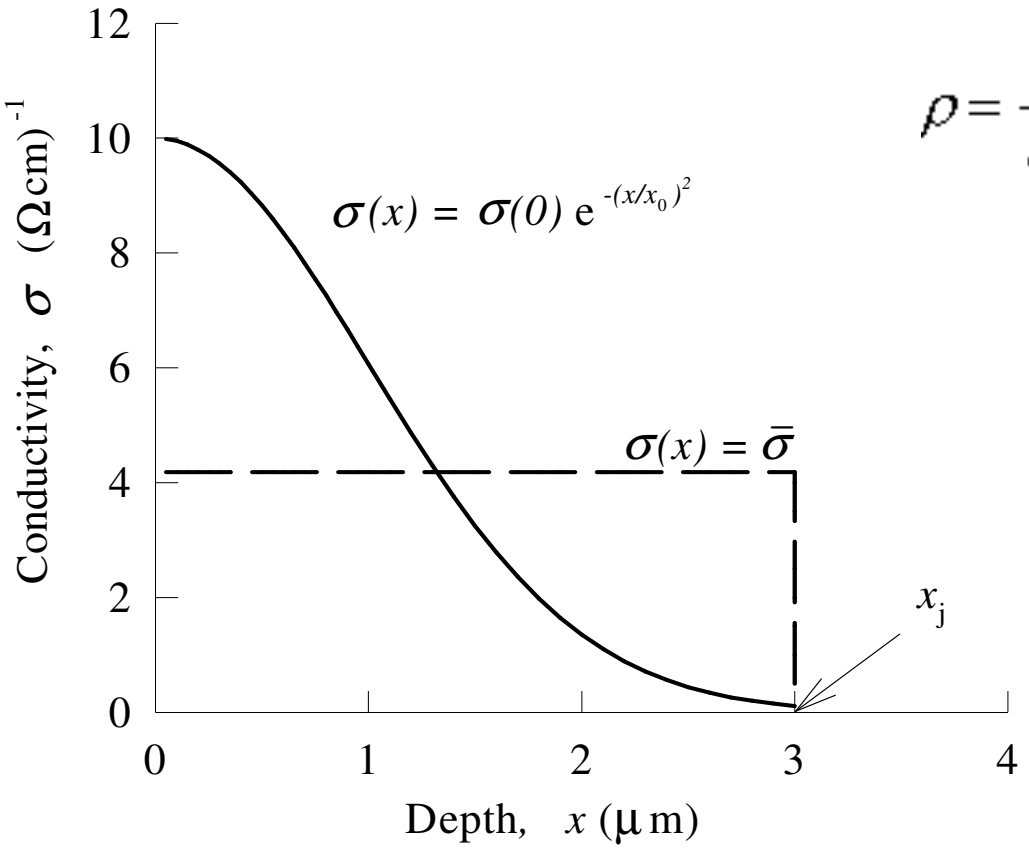
- Resistor
- Capacitor
- PN Diode
- MOS Structure
- MOS Transistor
- CMOS Transistors
- Bipolar Transistors
- Memories

Resistor



$$R_S = \frac{\rho}{t} \qquad R = R_S \frac{W}{L}$$

Conductivity

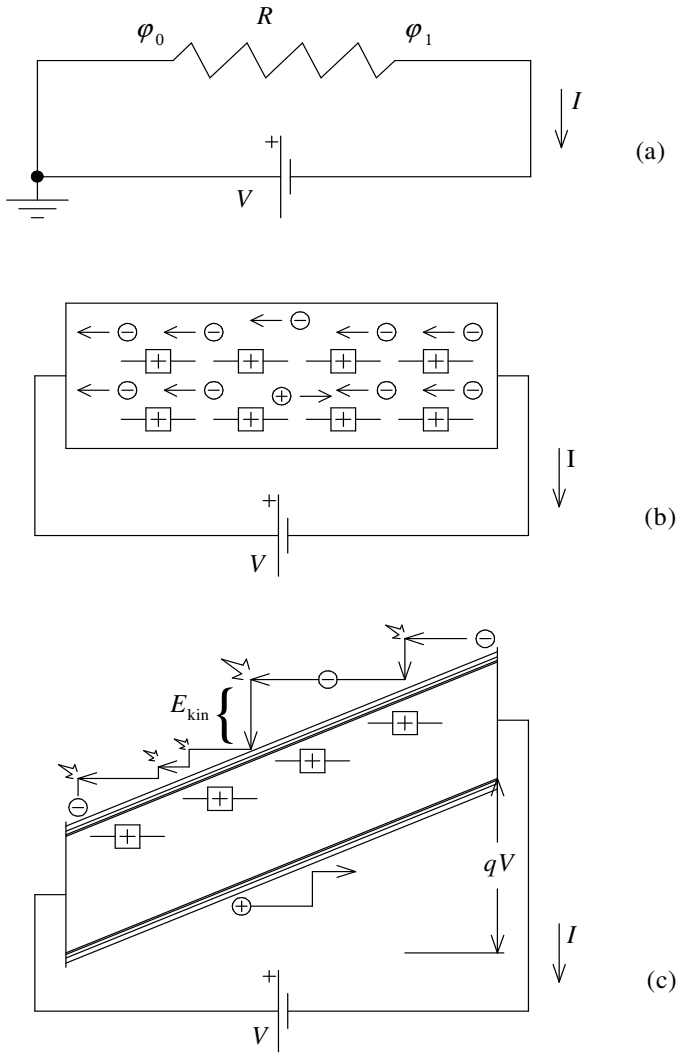


$$\rho = \frac{1}{\sigma} = \frac{1}{q(\mu_n n + \mu_p p)}$$

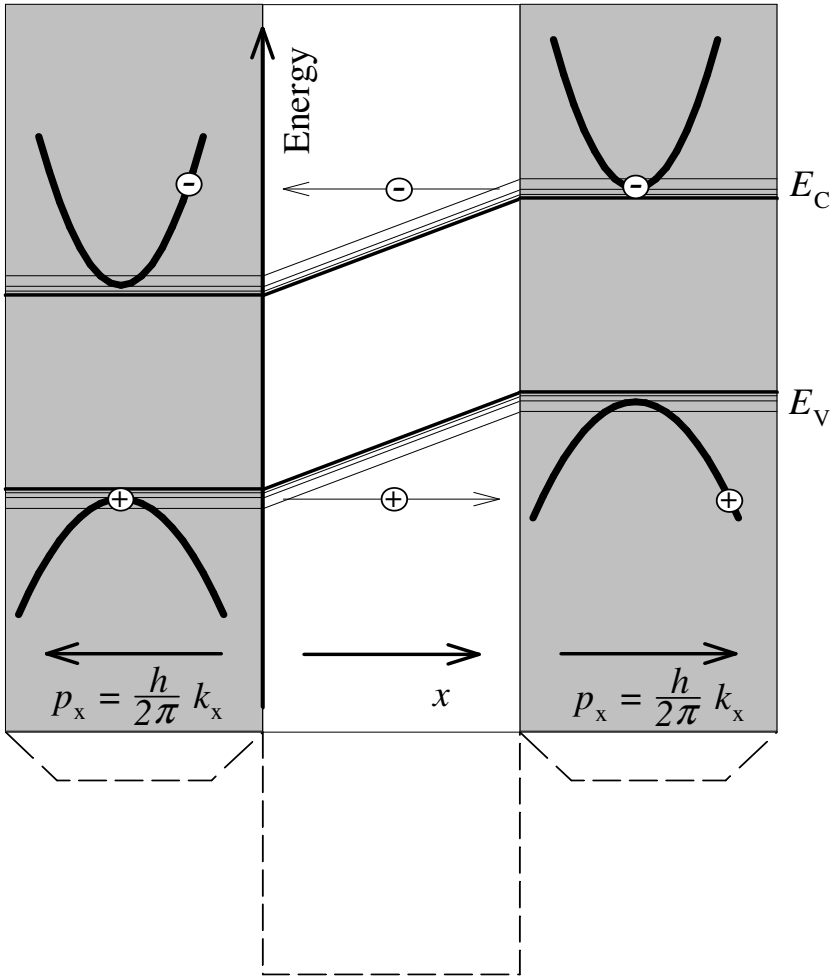
$$\mu_n = \frac{q}{KT} D_n$$

$$\mu_p = \frac{q}{KT} D_p$$

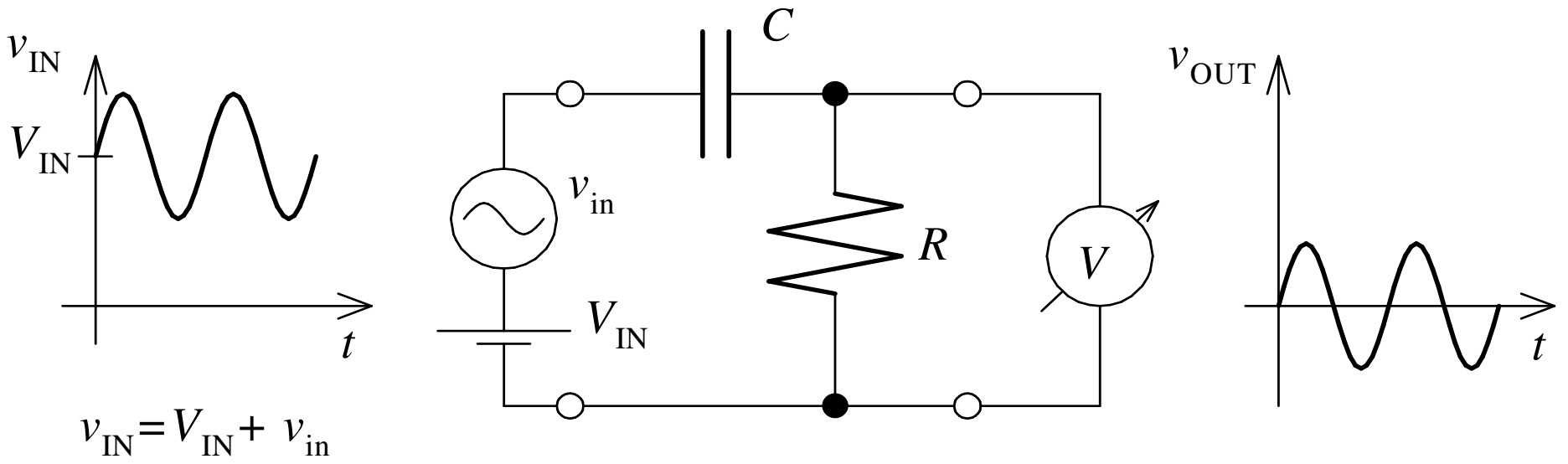
Electrical Current in Semiconductor (1)



Electrical Current in Semiconductor (2)

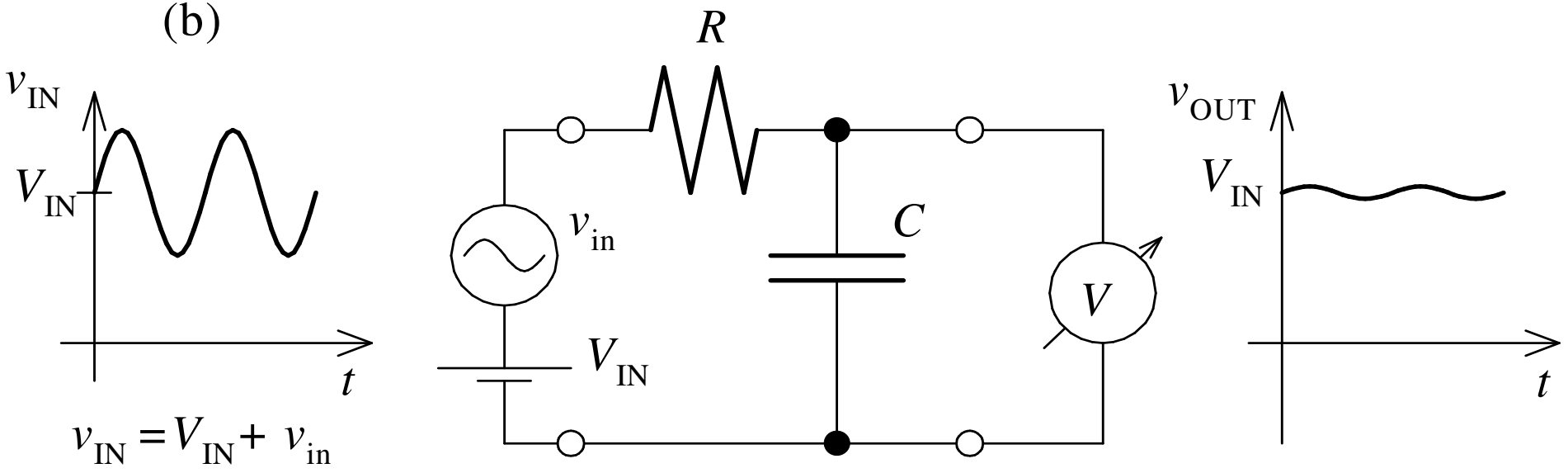


(a)



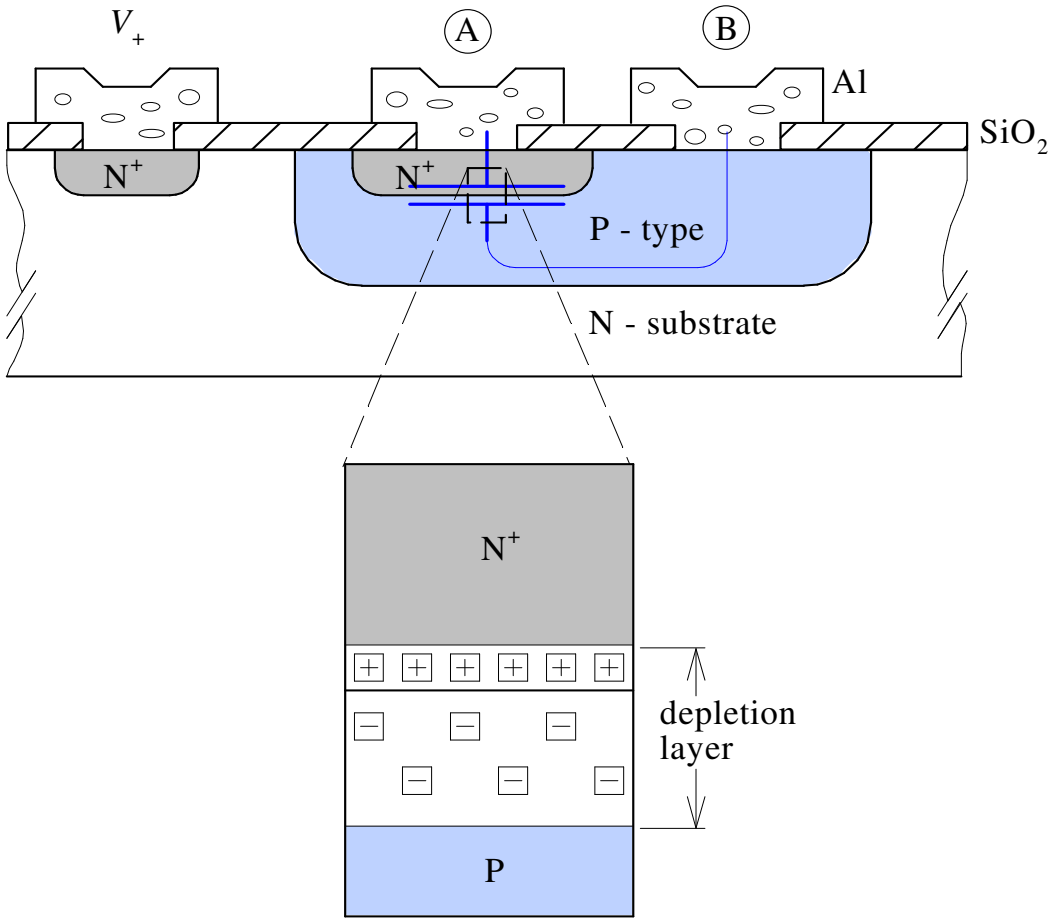
$v_{IN} = V_{IN} + v_{in}$

(b)

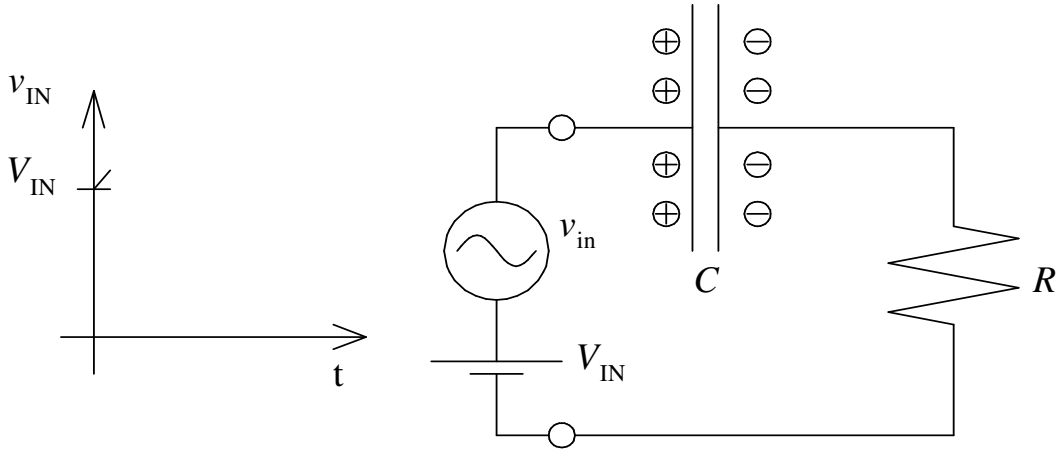


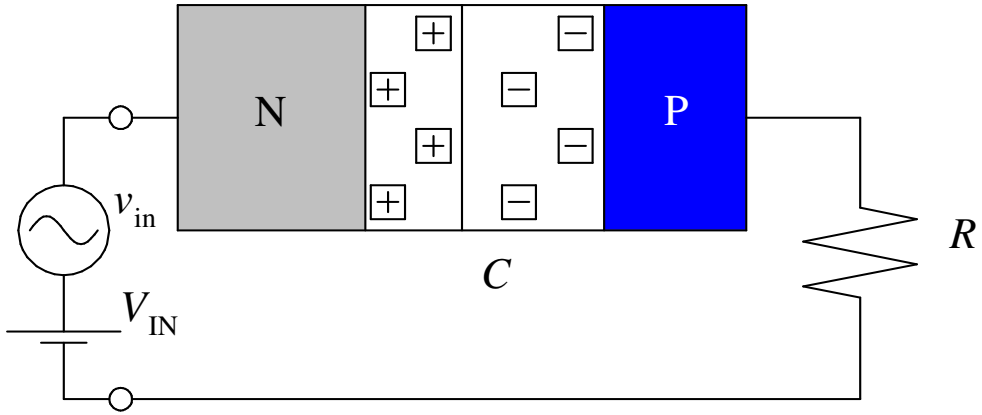
$v_{IN} = V_{IN} + v_{in}$

Capacitor

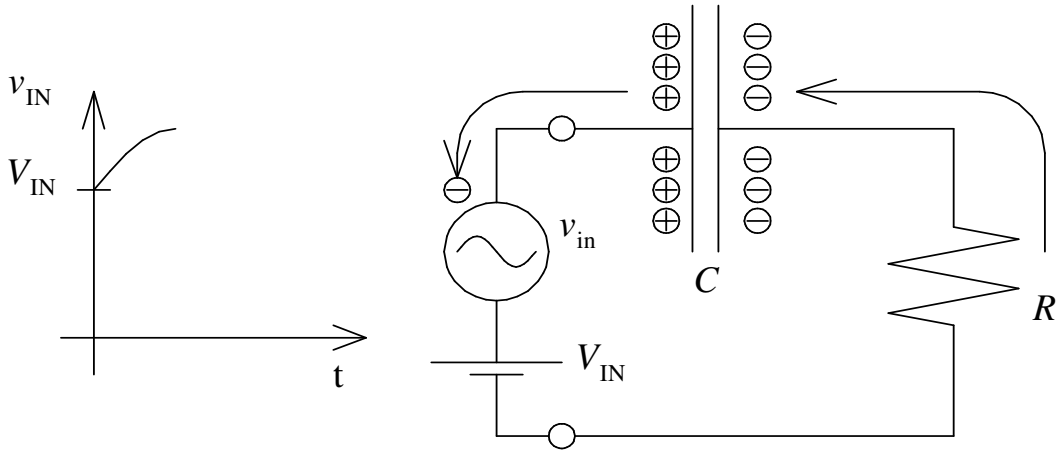


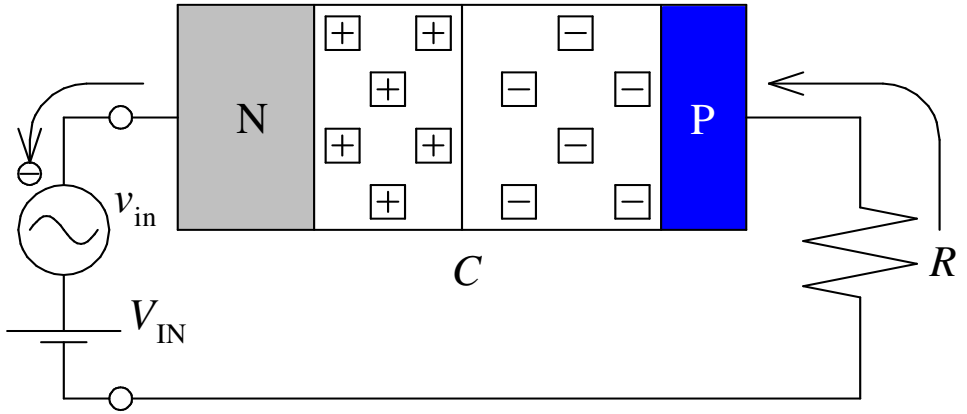
(a)


v_{IN}
V_{IN}
t
v_{in}
C
R
V_{IN}

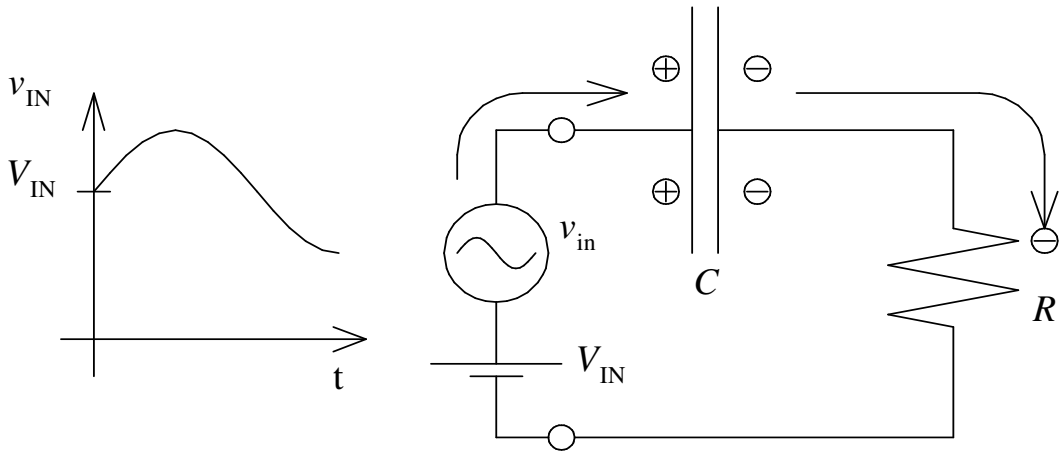

N
P
v_{in}
C
R
V_{IN}

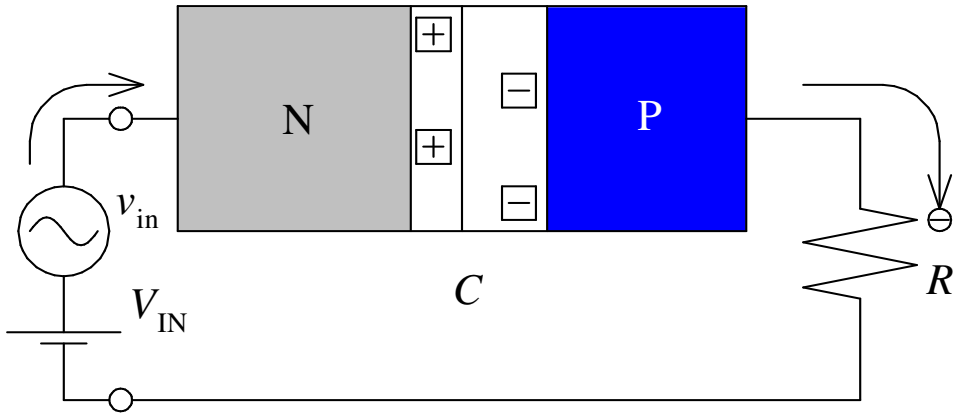
(b)


v_{IN}
V_{IN}
t
v_{in}
C
R
V_{IN}

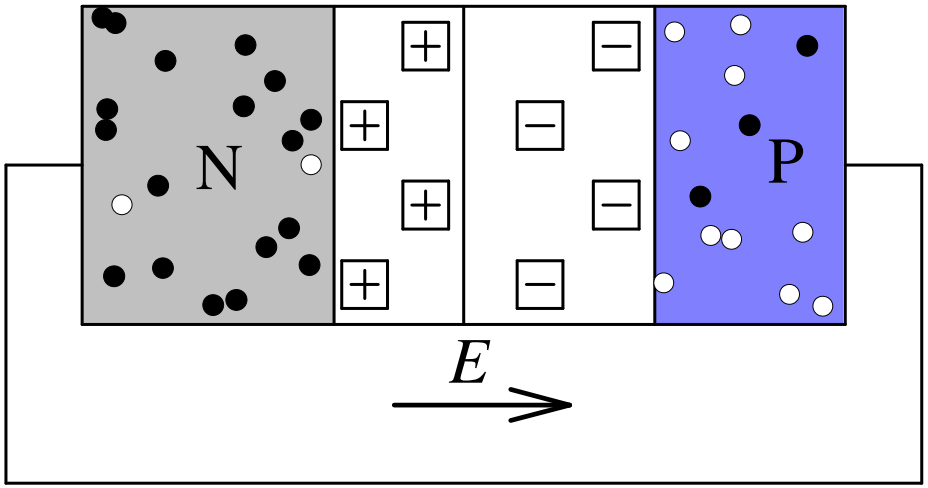

N
P
v_{in}
C
R
V_{IN}

(c)

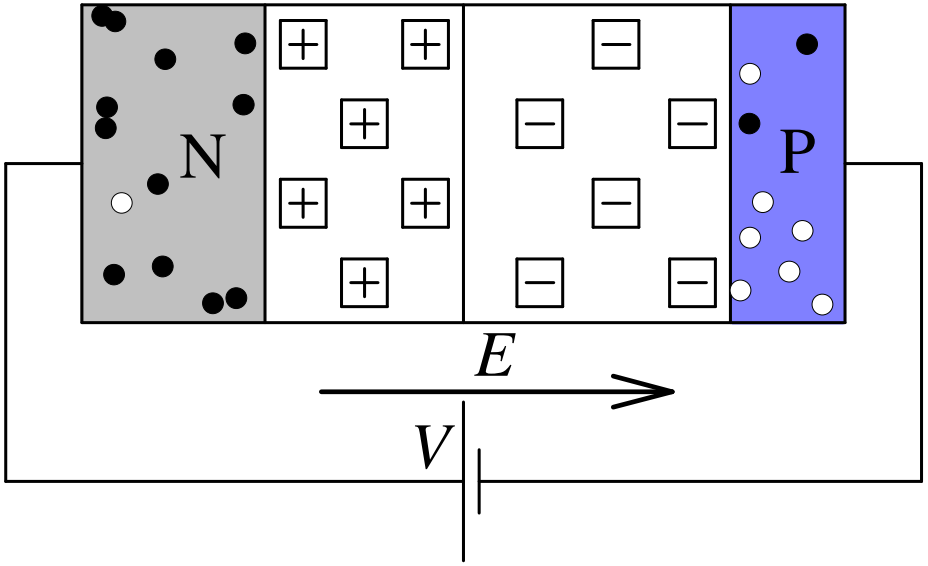

v_{IN}
V_{IN}
t
v_{in}
C
R
V_{IN}

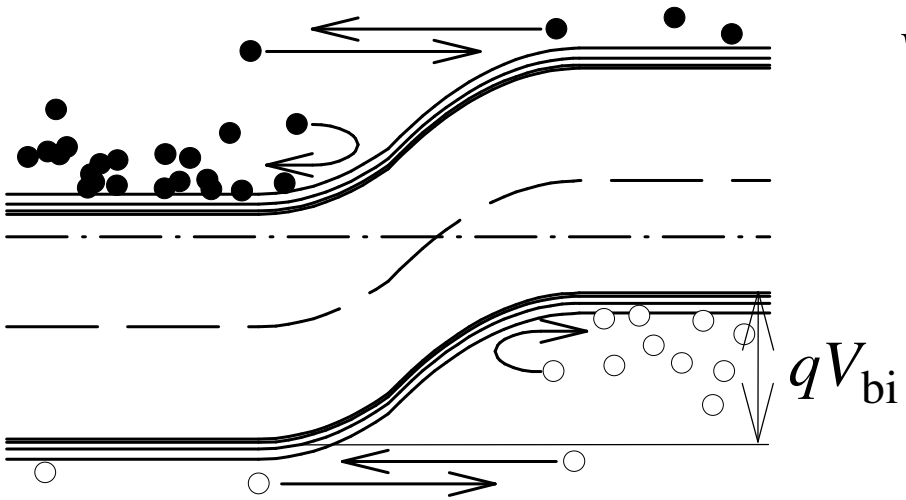

N
P
v_{in}
C
R
V_{IN}

zero bias

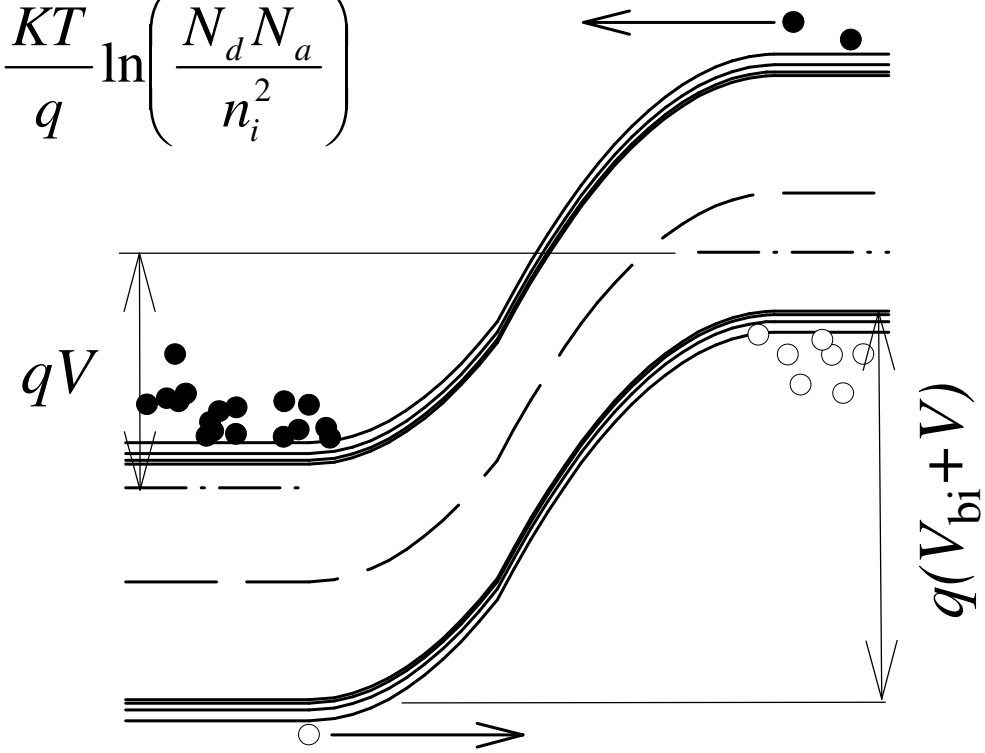


reverse bias





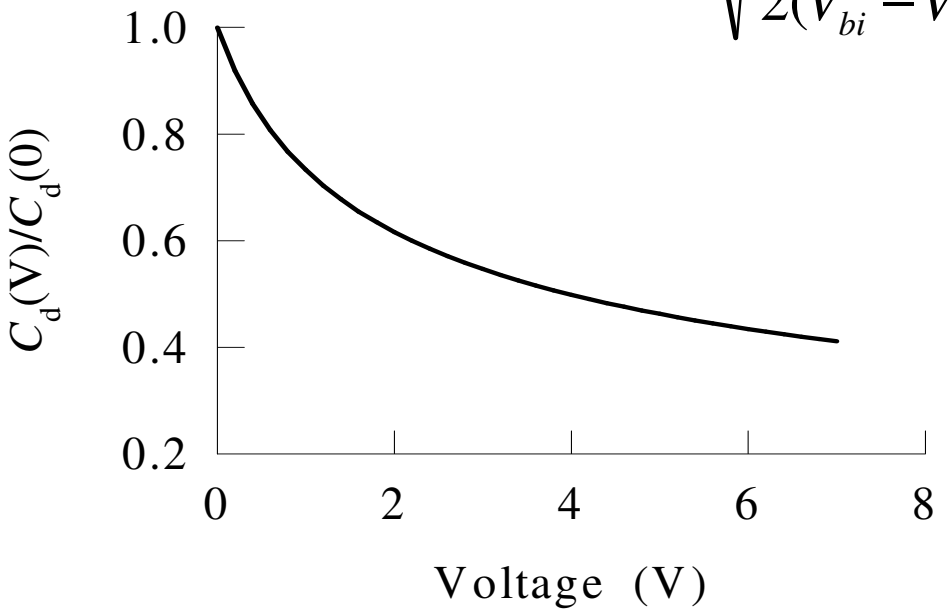
$$V_{bi} = \frac{KT}{q} \ln\left(\frac{N_d N_a}{n_i^2}\right)$$



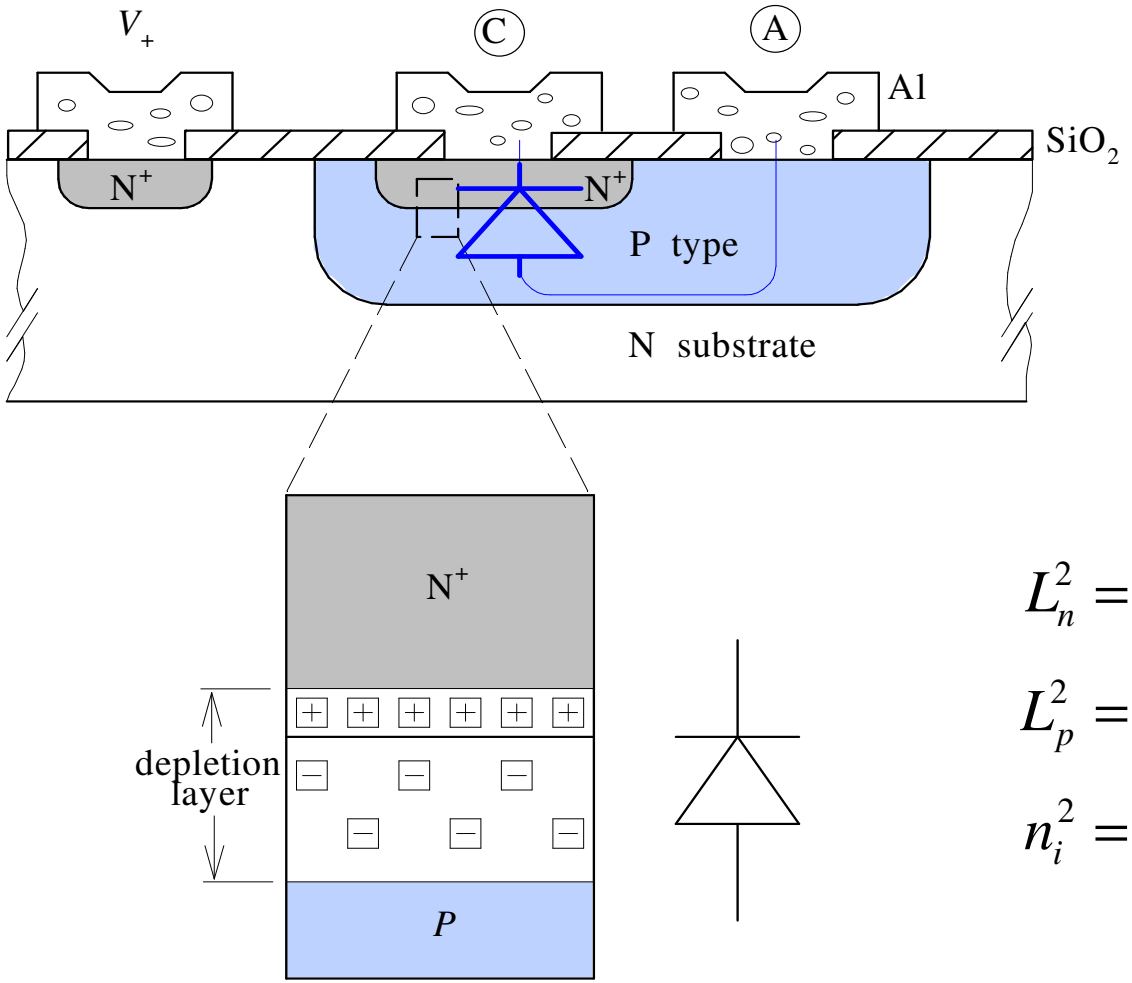
● electrons ○ holes

Depletion Layer Capacitance

$$C_d = S\sqrt{\frac{q\varepsilon_s}{2(V_{bi}-V)}\frac{N_d N_a}{N_d + N_a}}$$



PN Diode

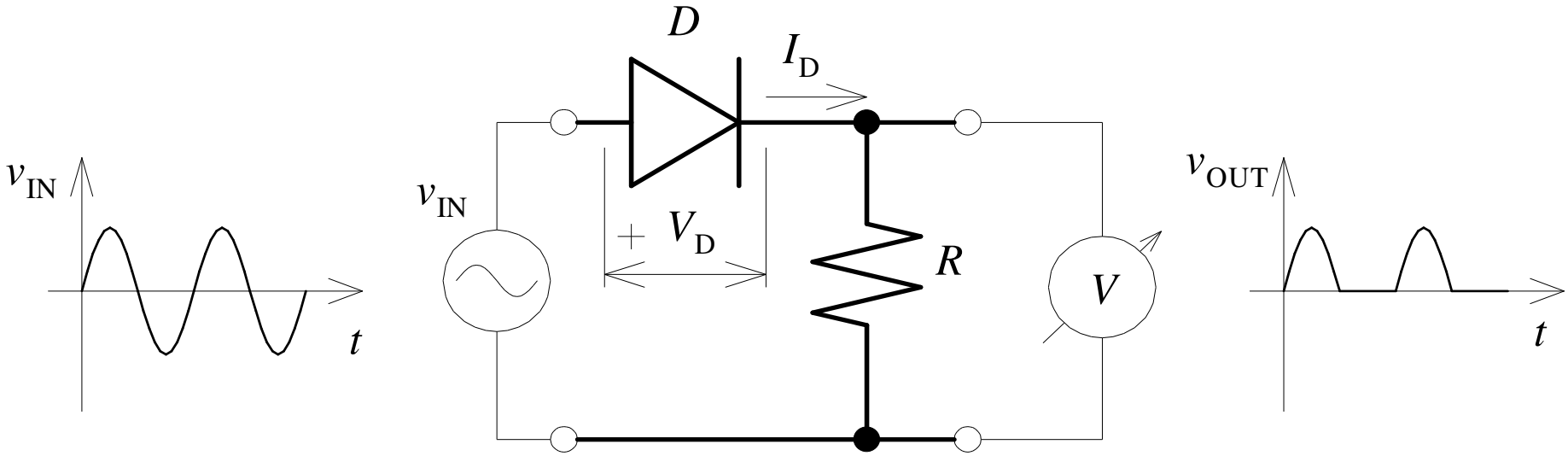


$$L_n^2 = D_n \tau_n$$

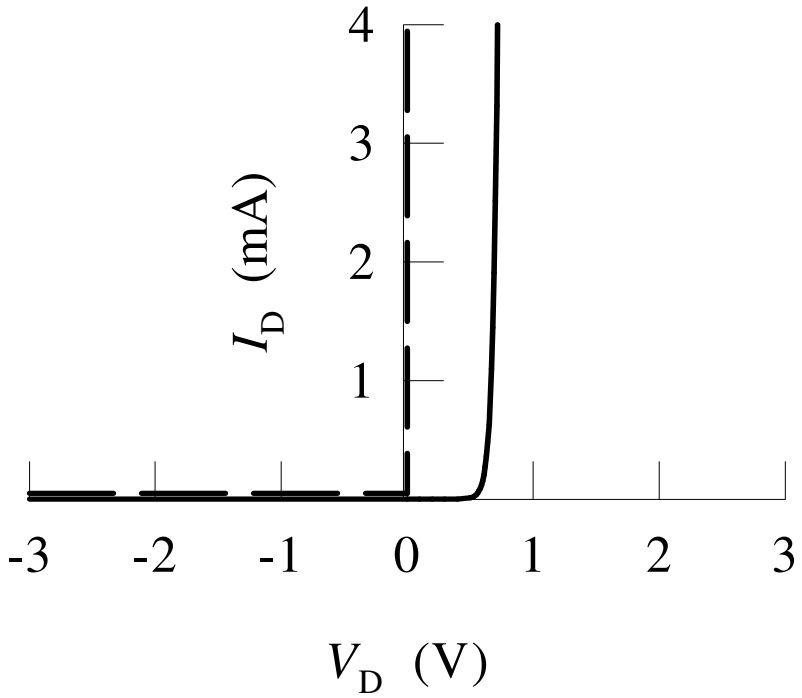
$$L_p^2 = D_p \tau_p$$

$$n_i^2 = np$$

(a)

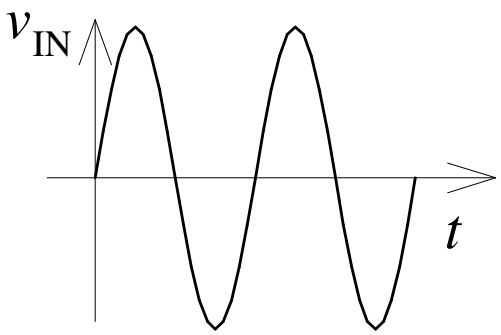


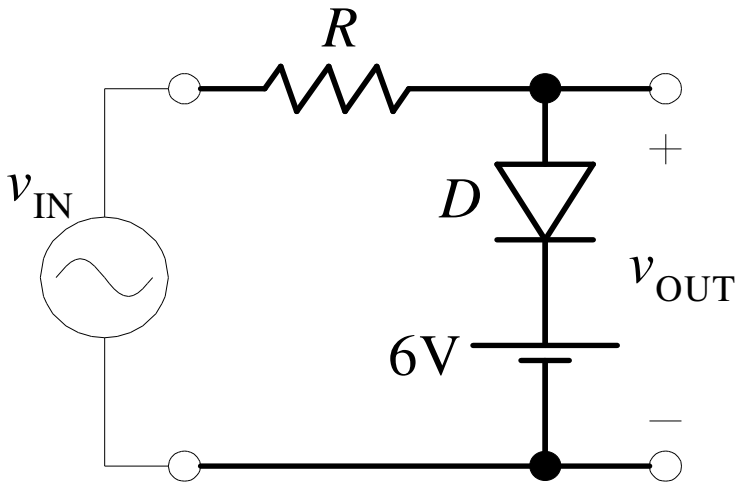
(b)

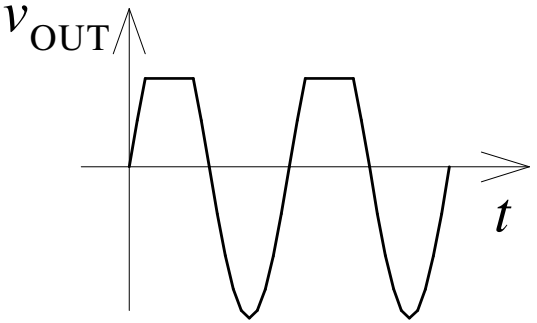


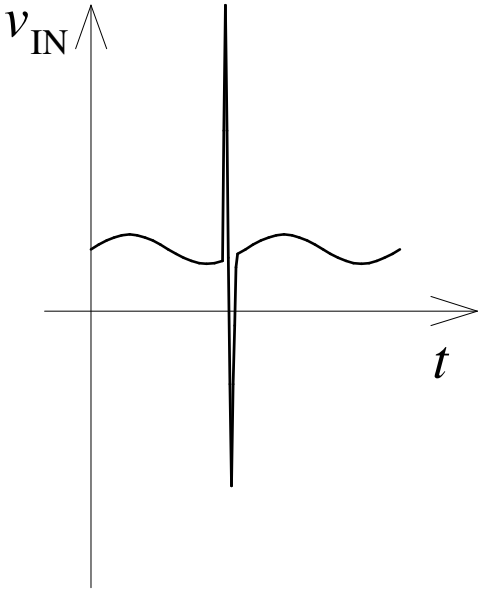
$$I_D = I_S\left(e^{\frac{qV_D}{KT}} - 1\right)$$

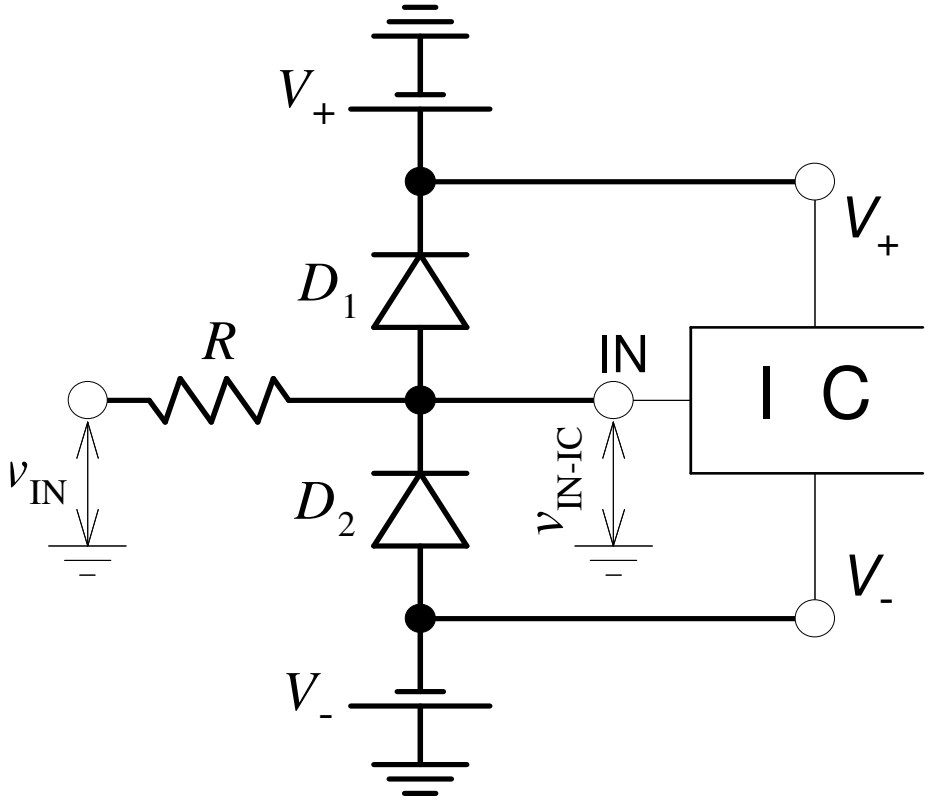
$$I_S = qS\left(\frac{L_n n_{p0}}{\tau_n} + \frac{L_p p_{n0}}{\tau_p}\right)$$

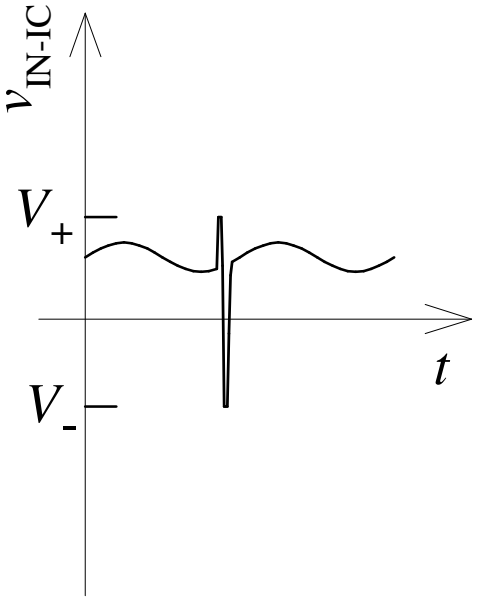

v_{IN}
t


R
v_{IN}
D
+
v_{OUT}
6V
–

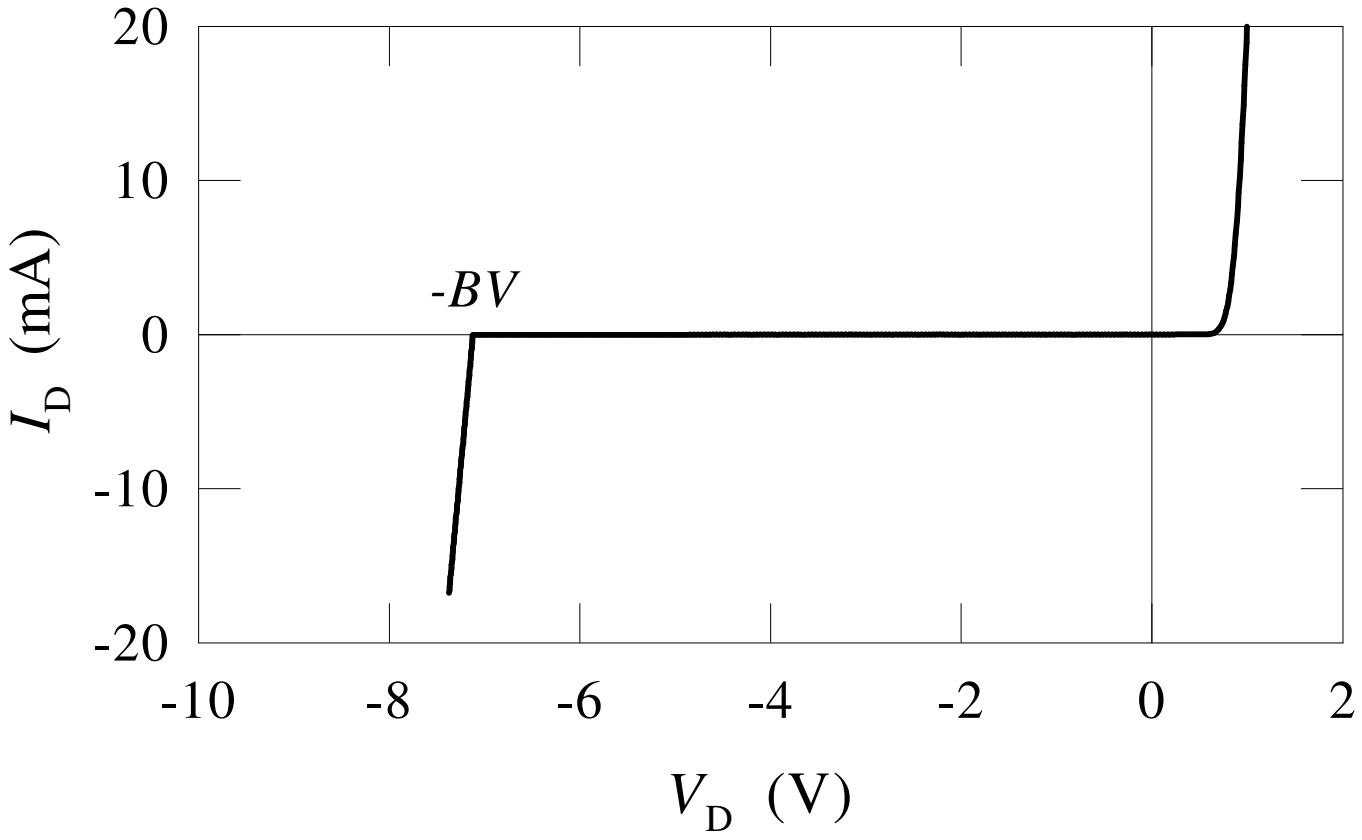

v_{OUT}
t


v_{IN}
t

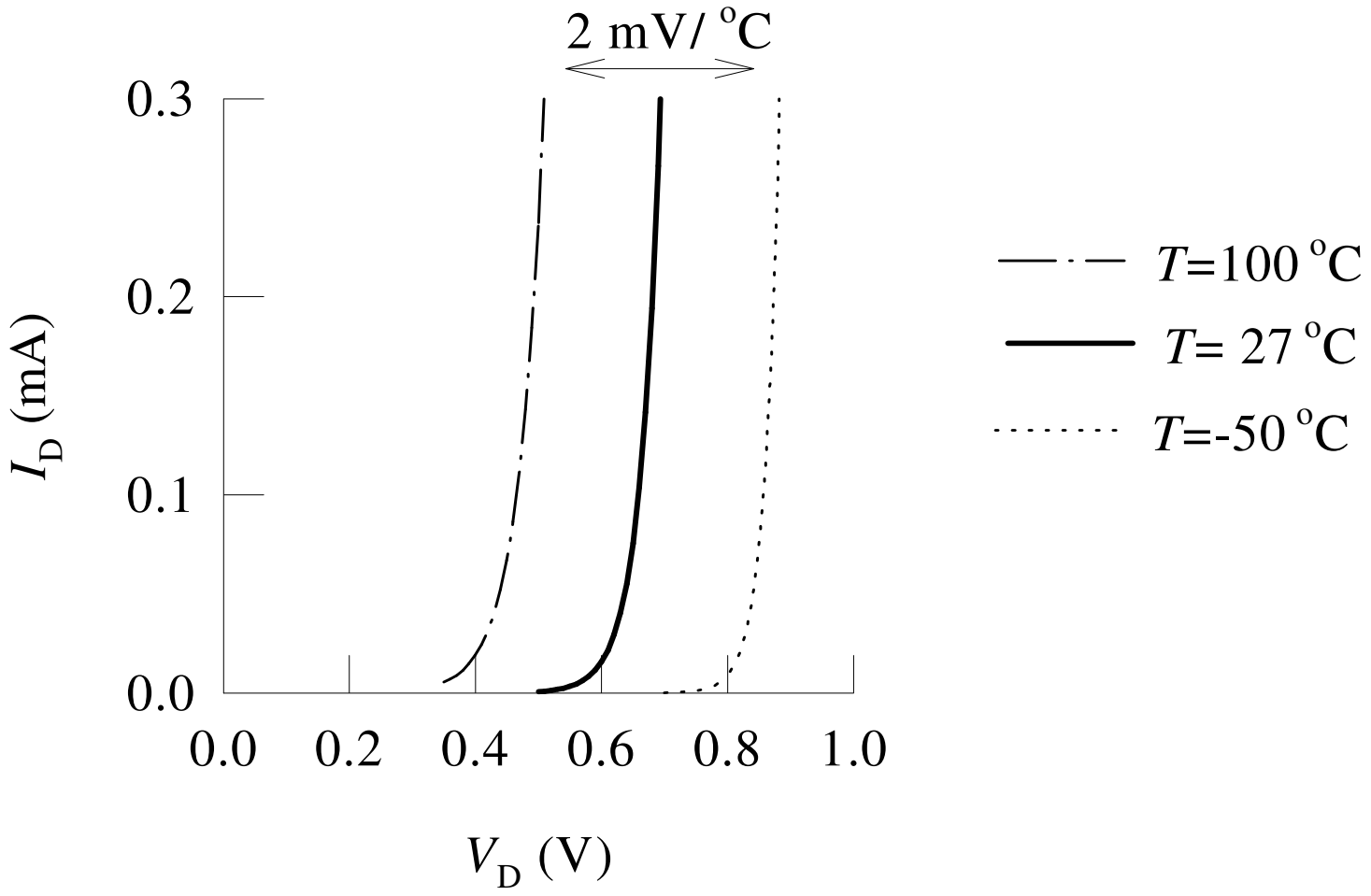

V_+
V_+
D_1
R
IN
I C
v_{IN}
v_{IN-IC}
D_2
V_-
V_-


v_{IN-IC}
V_+
V_-
t

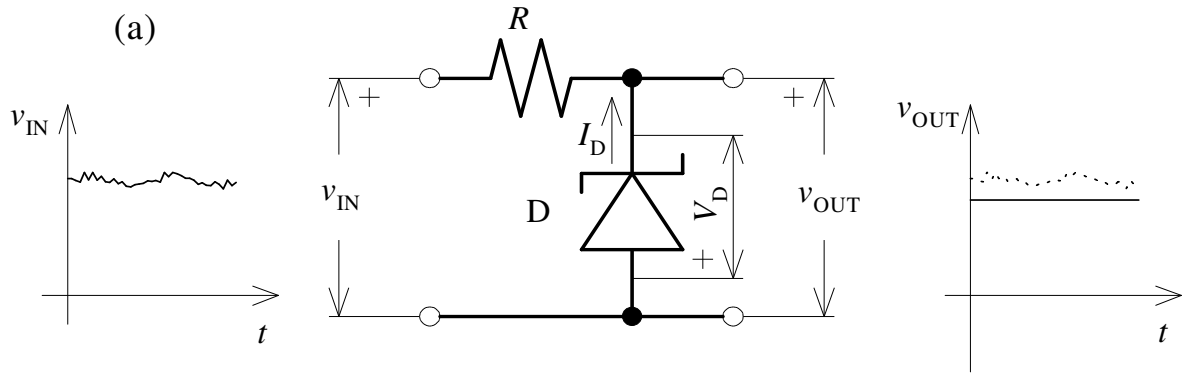
Diode Breakdown Voltage

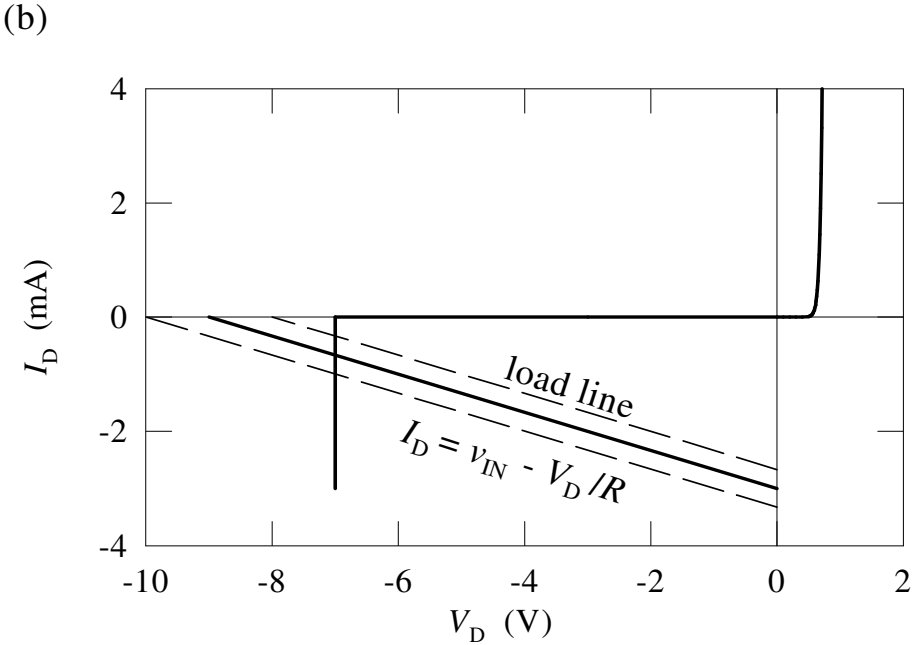


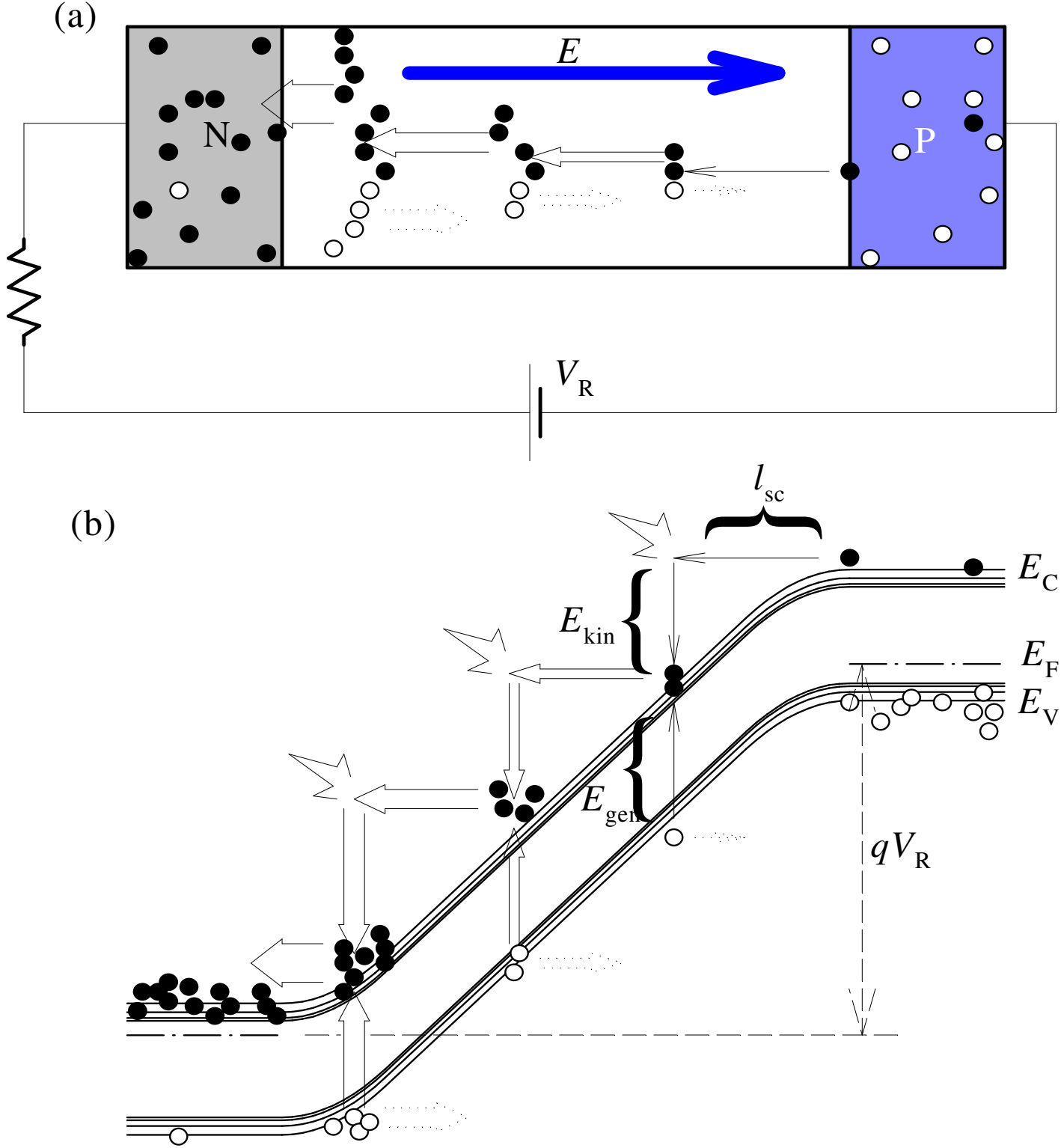
Temperature Dependence of I-V Characteristic



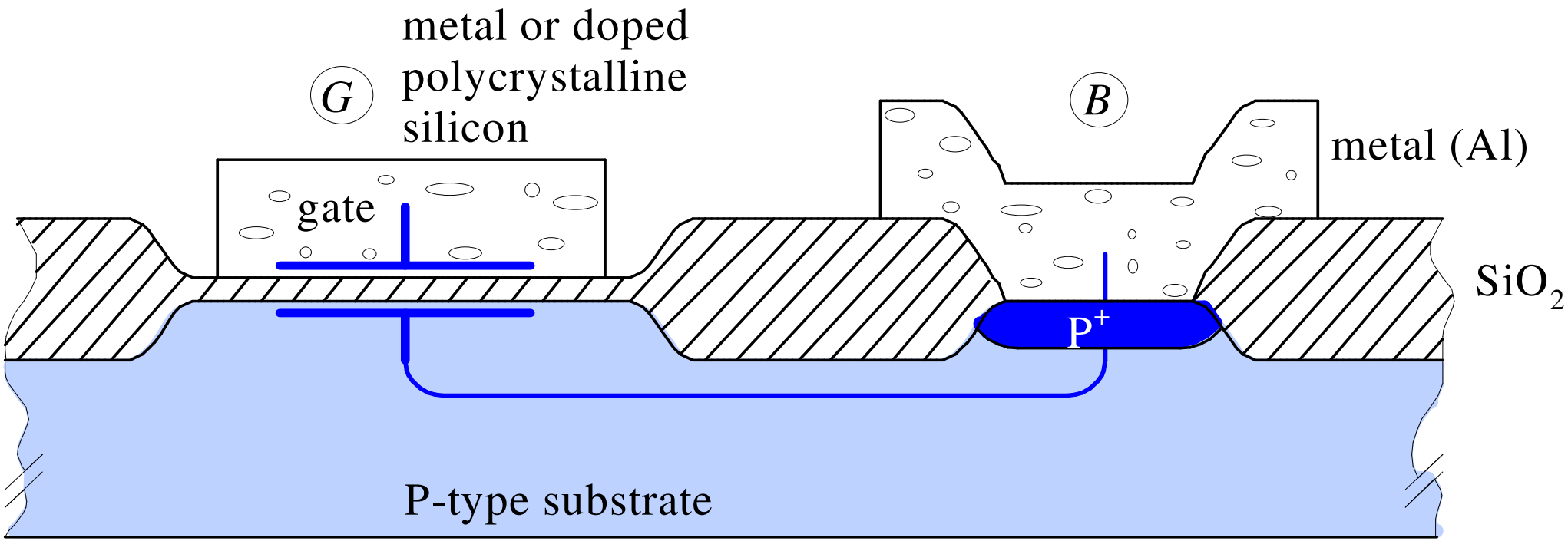
Zener Diode


(a)
R
v_{IN}
I_D
D
V_D
v_{OUT}
t

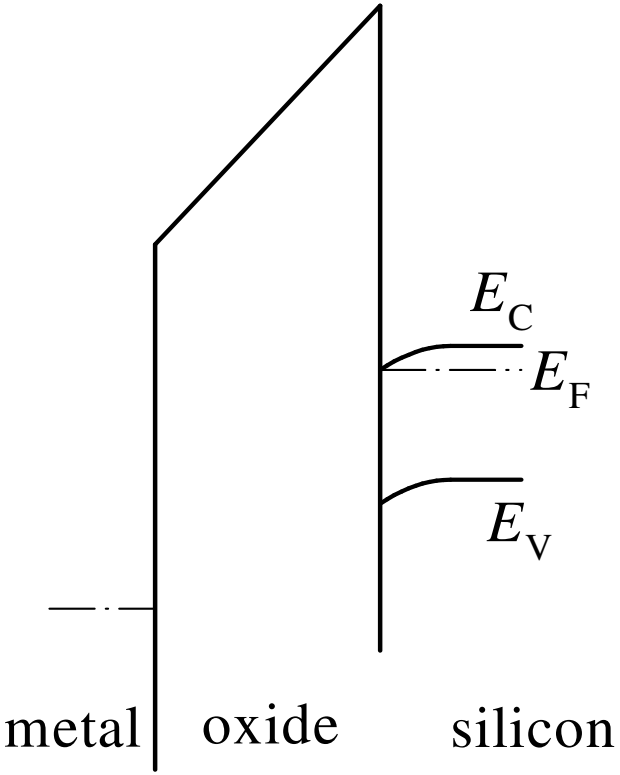

(b)
4
2
0
-2
-4
I_D (mA)
load line
$I_D = v_{IN} - V_D / R$
-10
-8
-6
-4
-2
0
2
V_D (V)

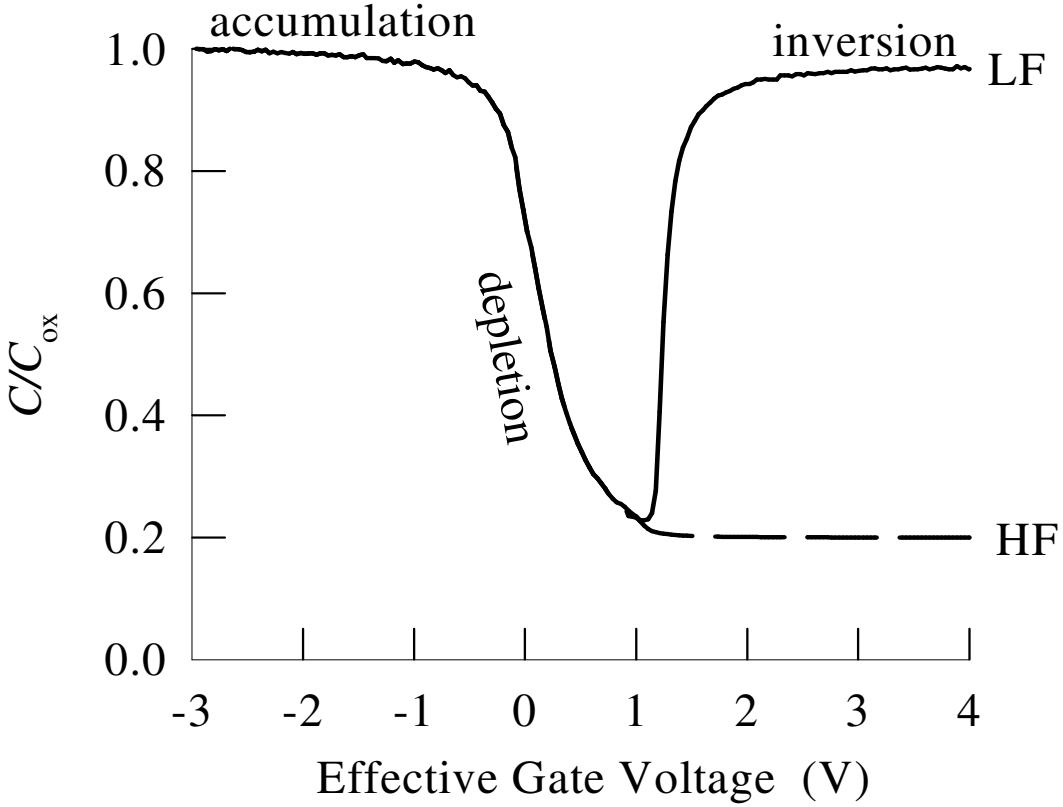

(a)
E
N
P
V_R
(b)
l_{sc}
E_C
E_{kin}
E_F
E_V
E_{gen}
qV_R

MOS Structure

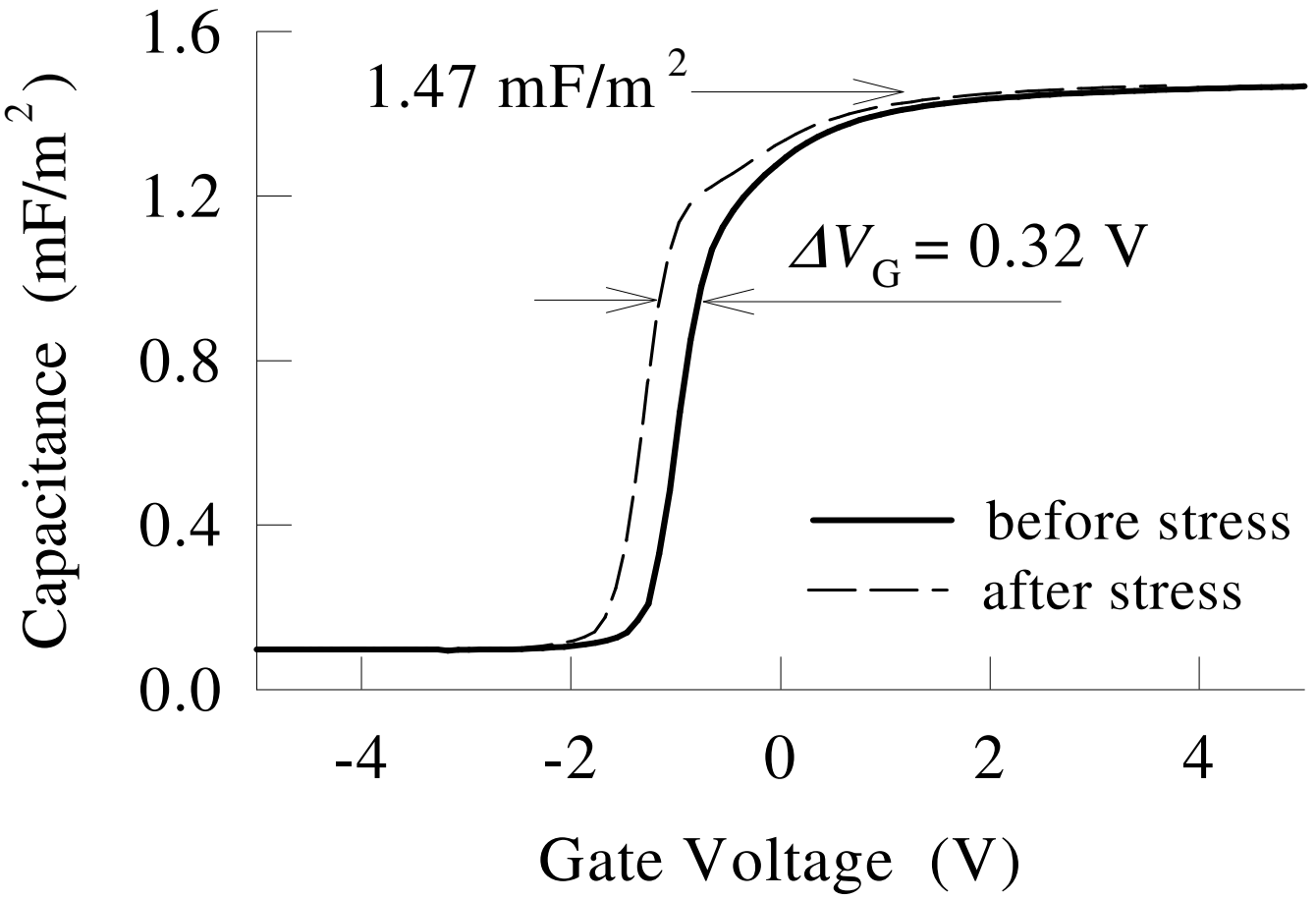


Energy Diagram and C-V Characteristic

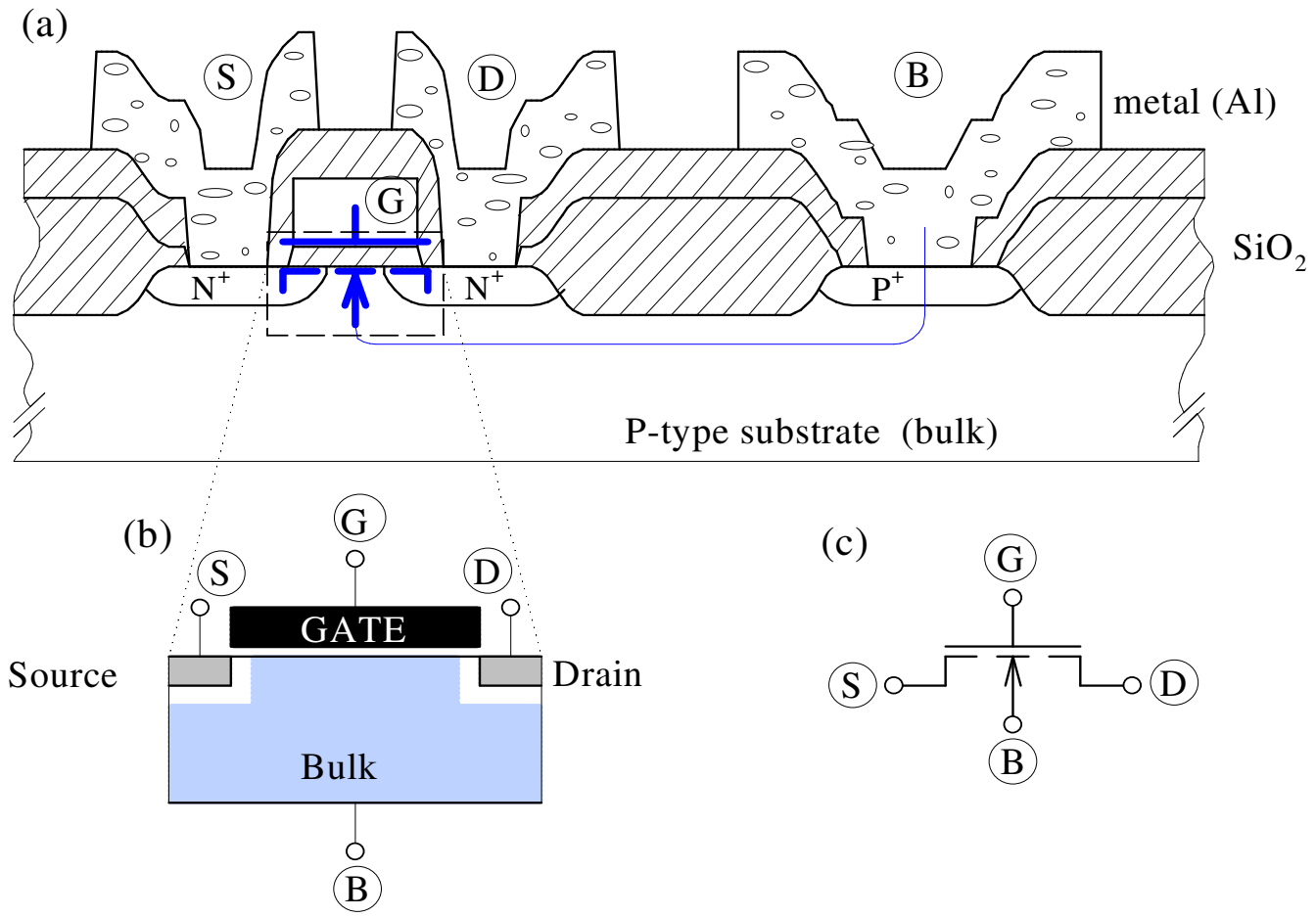




MOS Capacitance



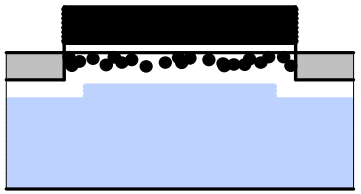
MOS Transistor



Input Threshold Voltage (1)

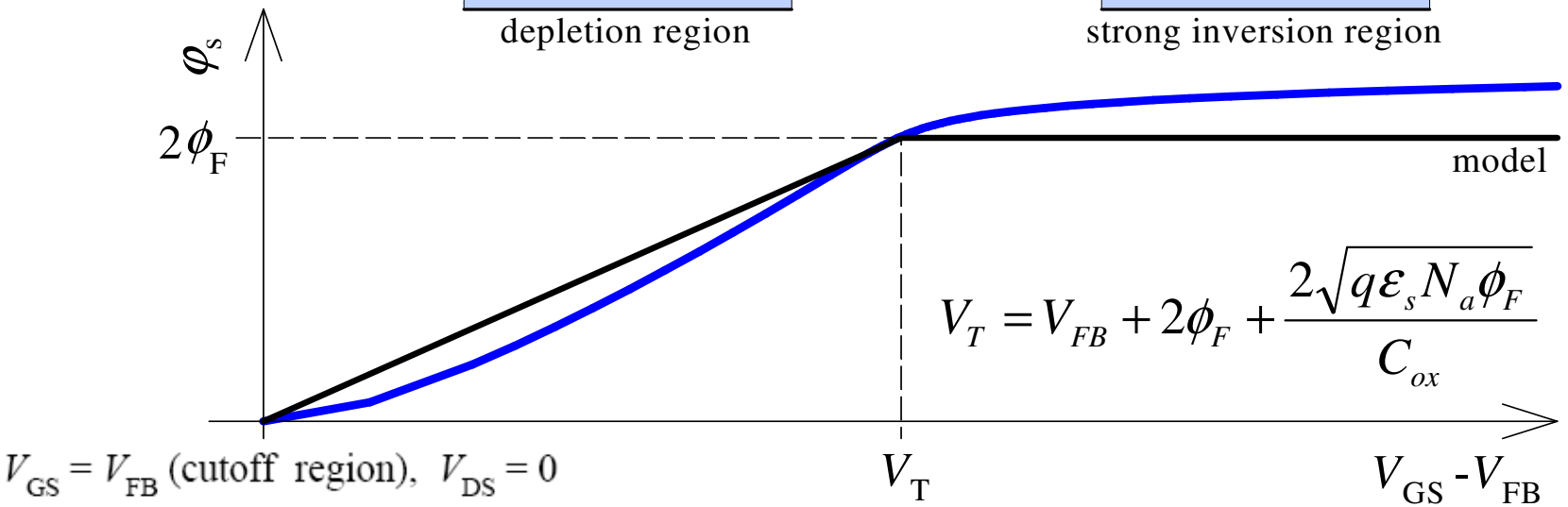
$$V_{GS} - V_{FB} - \varphi_S = \frac{Q_d}{C_{ox}}$$

depletion region



strong inversion region

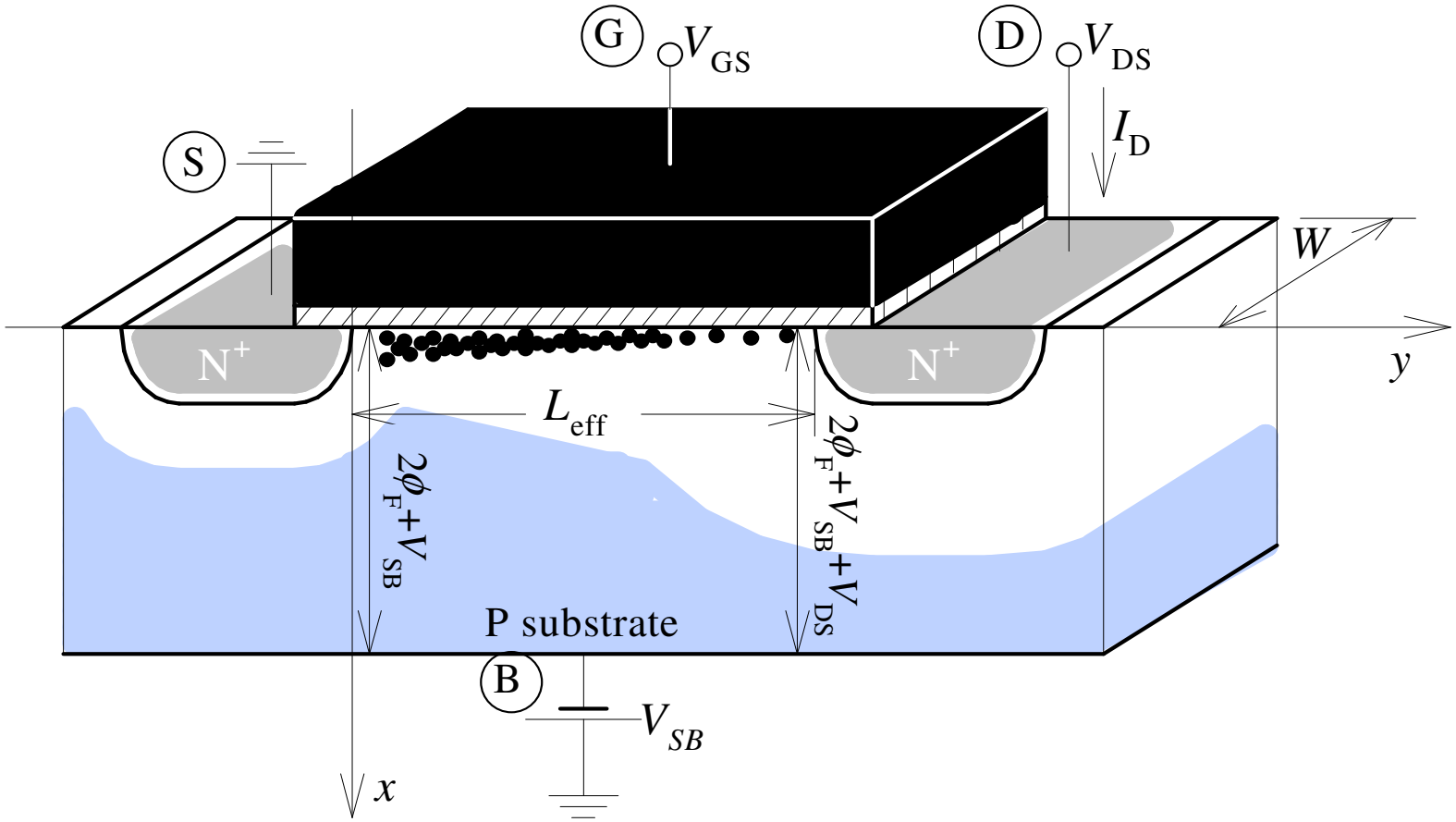
$$\varphi_S \approx 2\phi_F$$



flat bands

threshold voltage

Input Threshold Voltage (2)



Input Threshold Voltage (3)

$$C_{ox} = \varepsilon_{ox} / t_{ox} = 3.45 \times 10^{-3} \ F / m^2$$

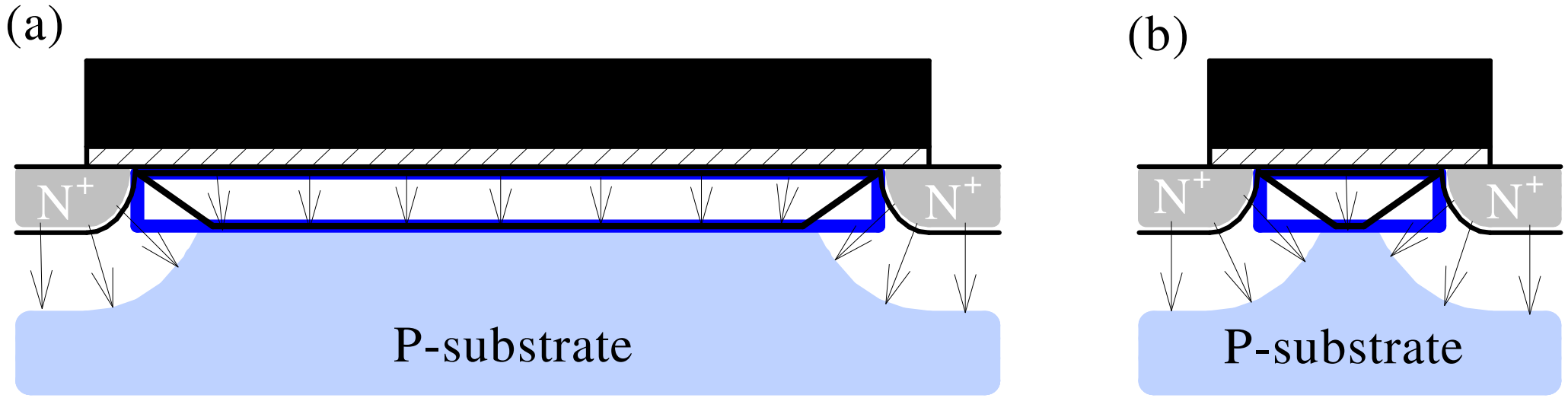
$$\phi_F = \frac{kT}{q} ln \frac{N_A}{n_i} = 0.401 V$$

$$\gamma = \frac{\sqrt{2\varepsilon_{si} q N_A}}{C_{ox}} = \frac{\sqrt{2 \cdot 11.8 \cdot 8.85 \times 10^{-12} \cdot 1.6 \times 10^{-19} \cdot 5 \times 10^{22}}}{3.45 \times 10^{-3}} = 0.375 \ V^{1/2}$$

$$V_T(0) = V_{FB} + 2\phi_F + \gamma \sqrt{2\phi_F + V_{SB}}$$

$$= -0.984 + 2 \cdot 0.401 + 0.375 \sqrt{2 \cdot 0.401 + 0} = 0.15 V$$

Input Threshold Voltage (4)



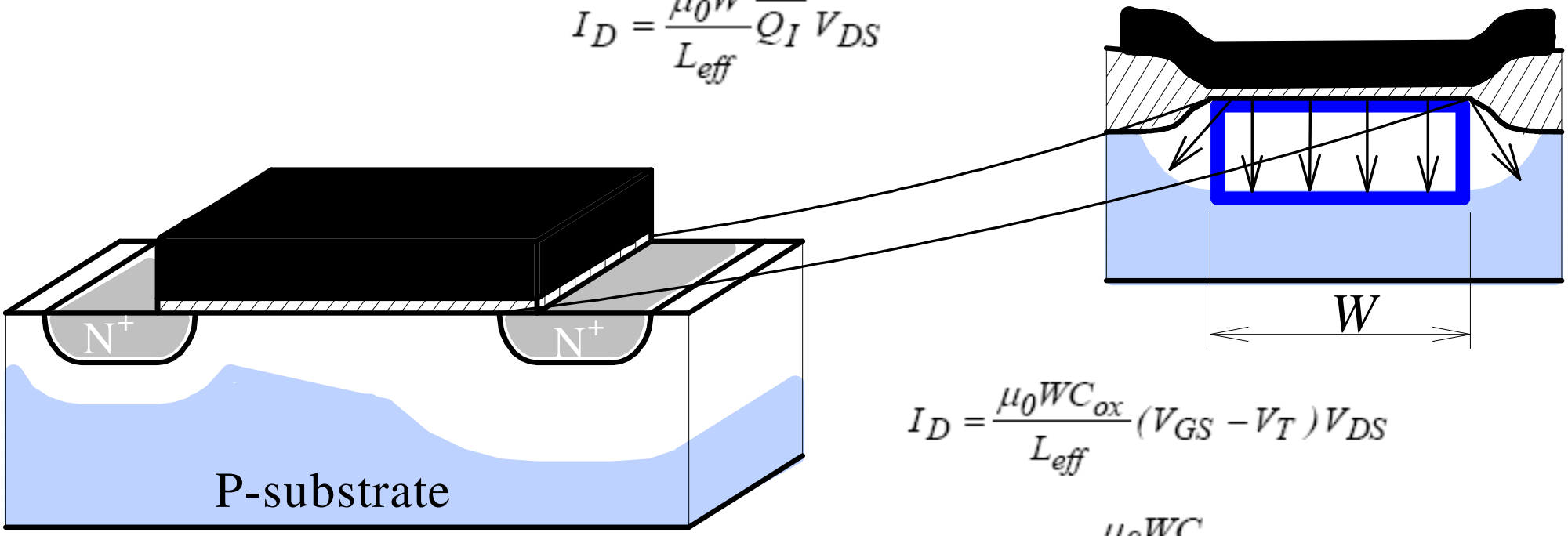
Output Current (1)

$$j = \sigma E$$

$$j = q \mu_0 n E$$

$$\underbrace{j\, x_{ch}\, W}_{I_D(A)} = \mu_0 \underbrace{q\, n\, x_{ch}}_{\overline{Q_I}\ (C/m^2)} W \underbrace{E}_{V_{DS}/L_{eff}}$$

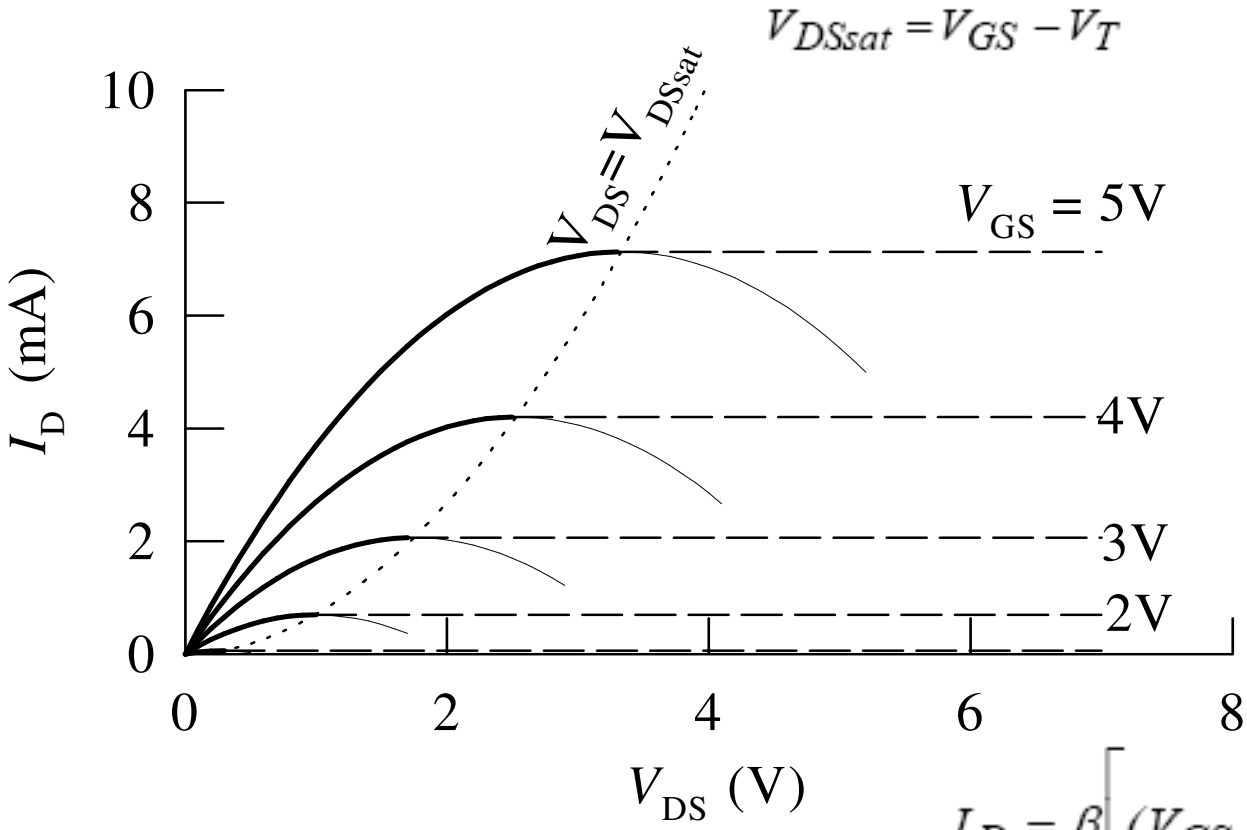
$$I_D = \frac{\mu_0 W}{L_{eff}} \overline{Q_I}\, V_{DS}$$



$$I_D = \frac{\mu_0 W C_{ox}}{L_{eff}} (V_{GS} - V_T) V_{DS}$$

$$\beta = \frac{\mu_0 W C_{ox}}{L_{eff}}$$

Output Current (2)



V_{FB} = -1.0V

$2\phi_F$ = 0.75V

γ = 0.95V$^{1/2}$

β = 1.0mA/V^2

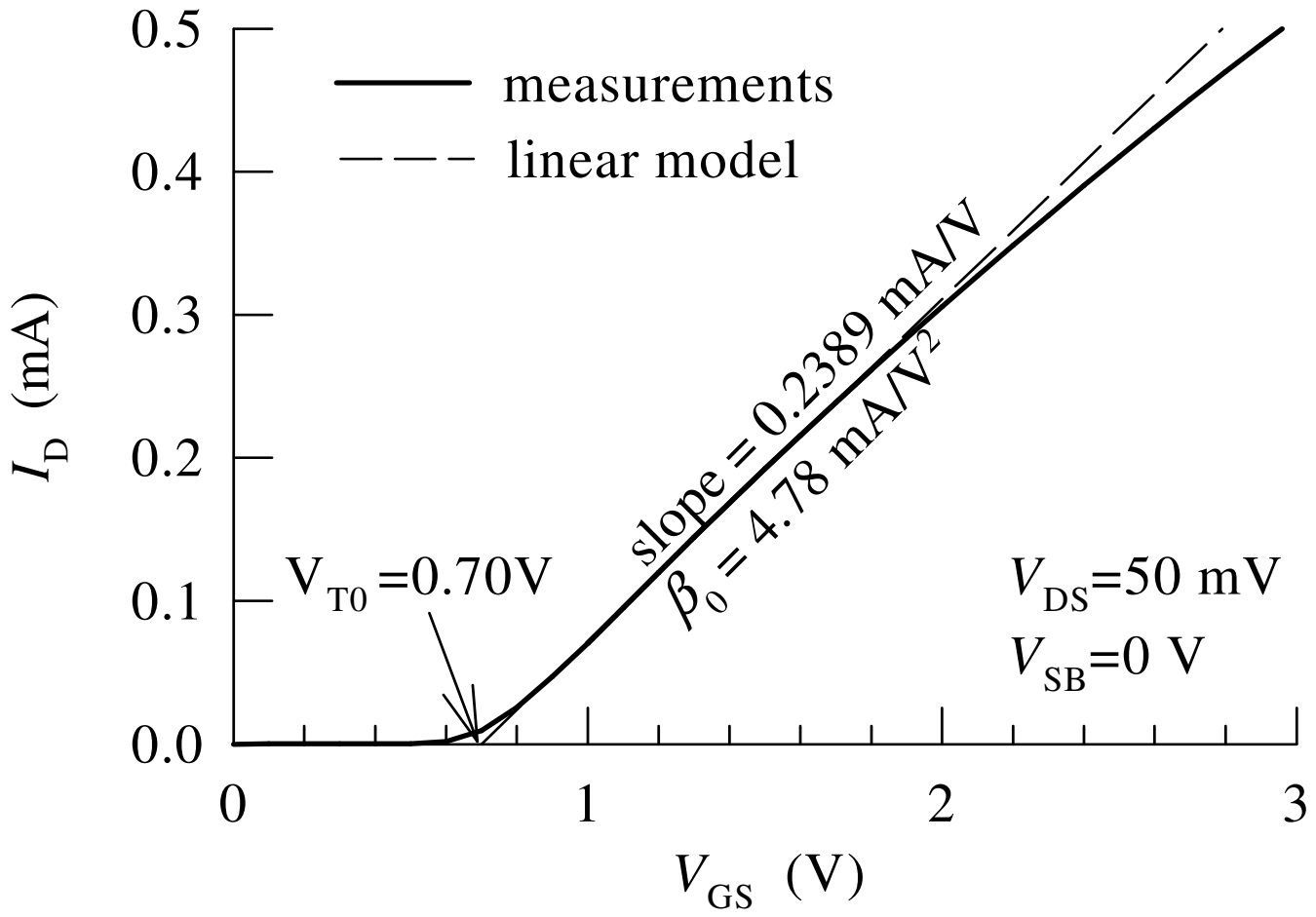
$$I_D = \beta\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right], \quad 0 \le V_{DS} < V_{DSsat}$$

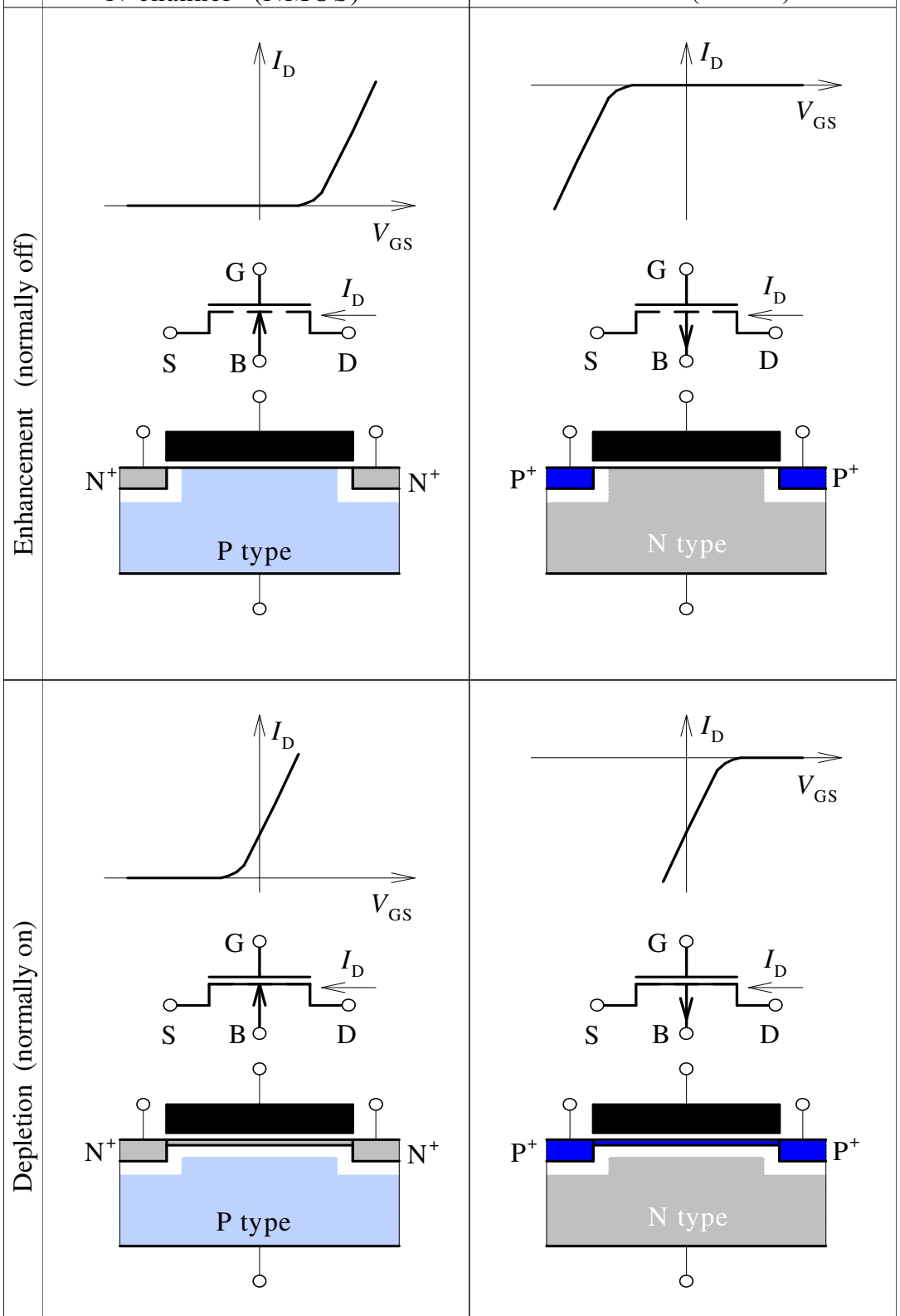
$$I_D = \frac{\beta}{2}(V_{GS} - V_T)^2, \quad V_{DS} \ge V_{DSsat}$$

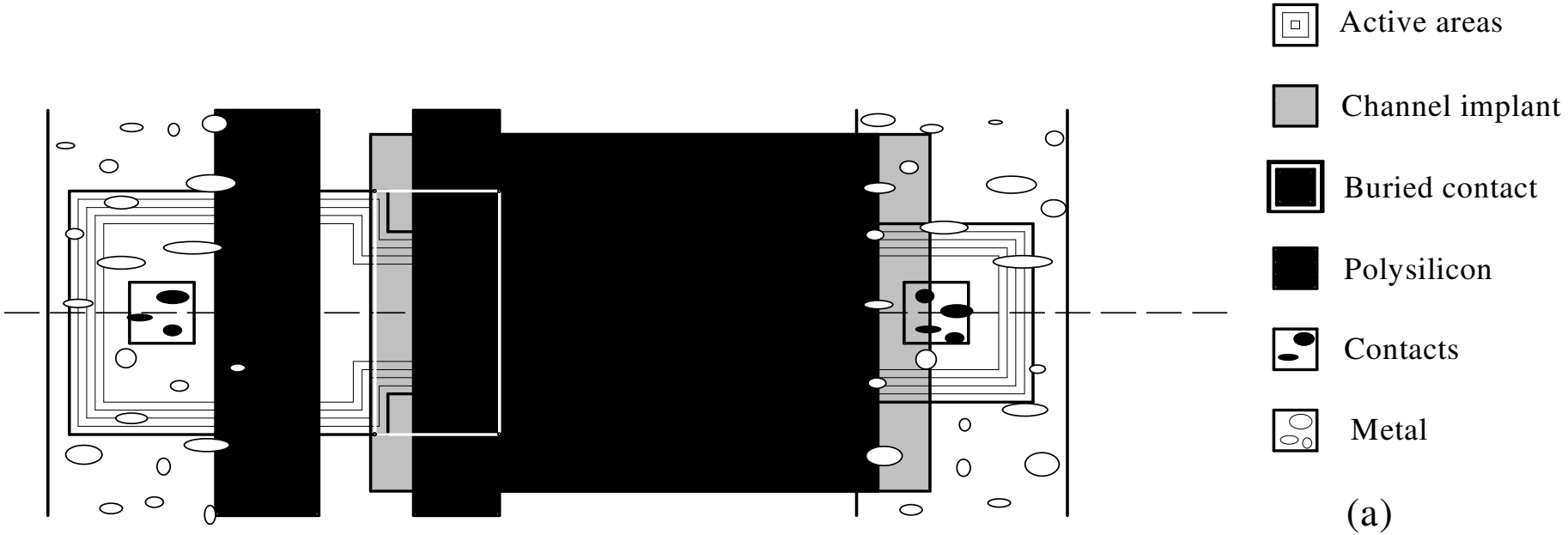
solid lines: equation

dashed lines: saturation current

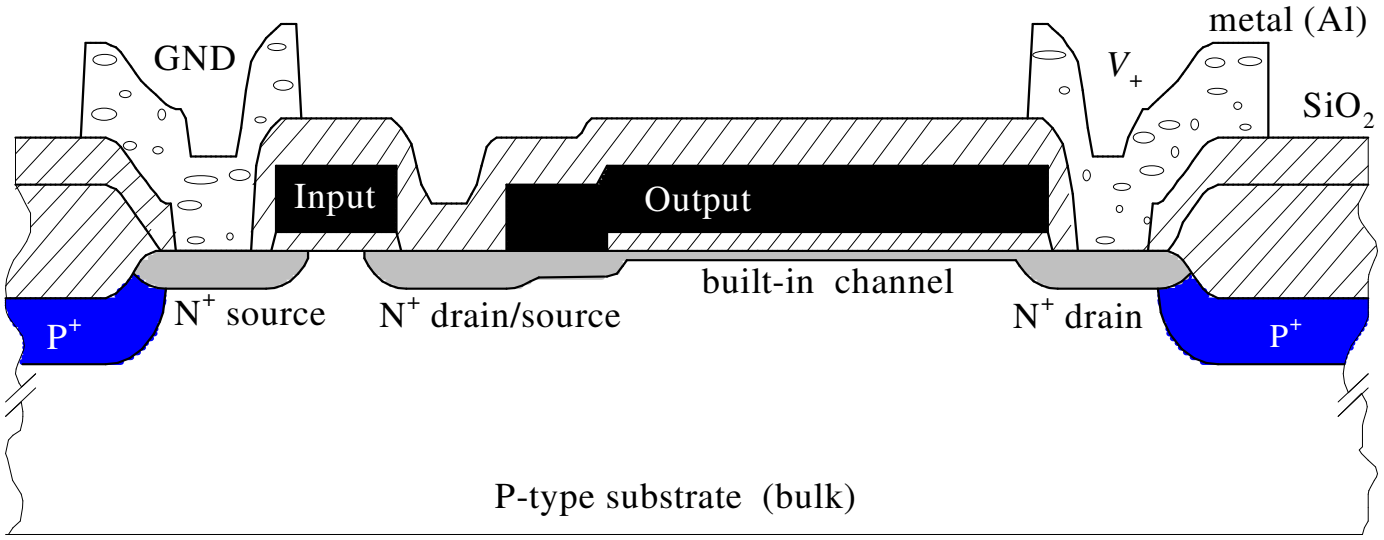
Output Current (3)



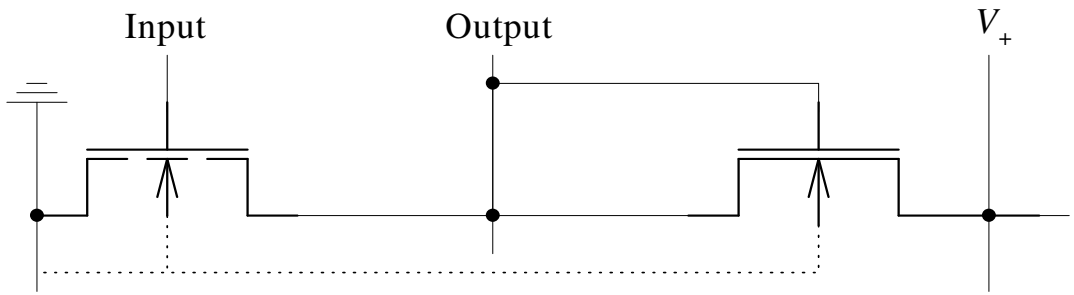

Enhancement (normally off)
Depletion (normally on)
I_D
V_{GS}
G
S
B
D
N^+
P^+
P type
N type


Active areas
Channel implant
Buried contact
Polysilicon
Contacts
Metal

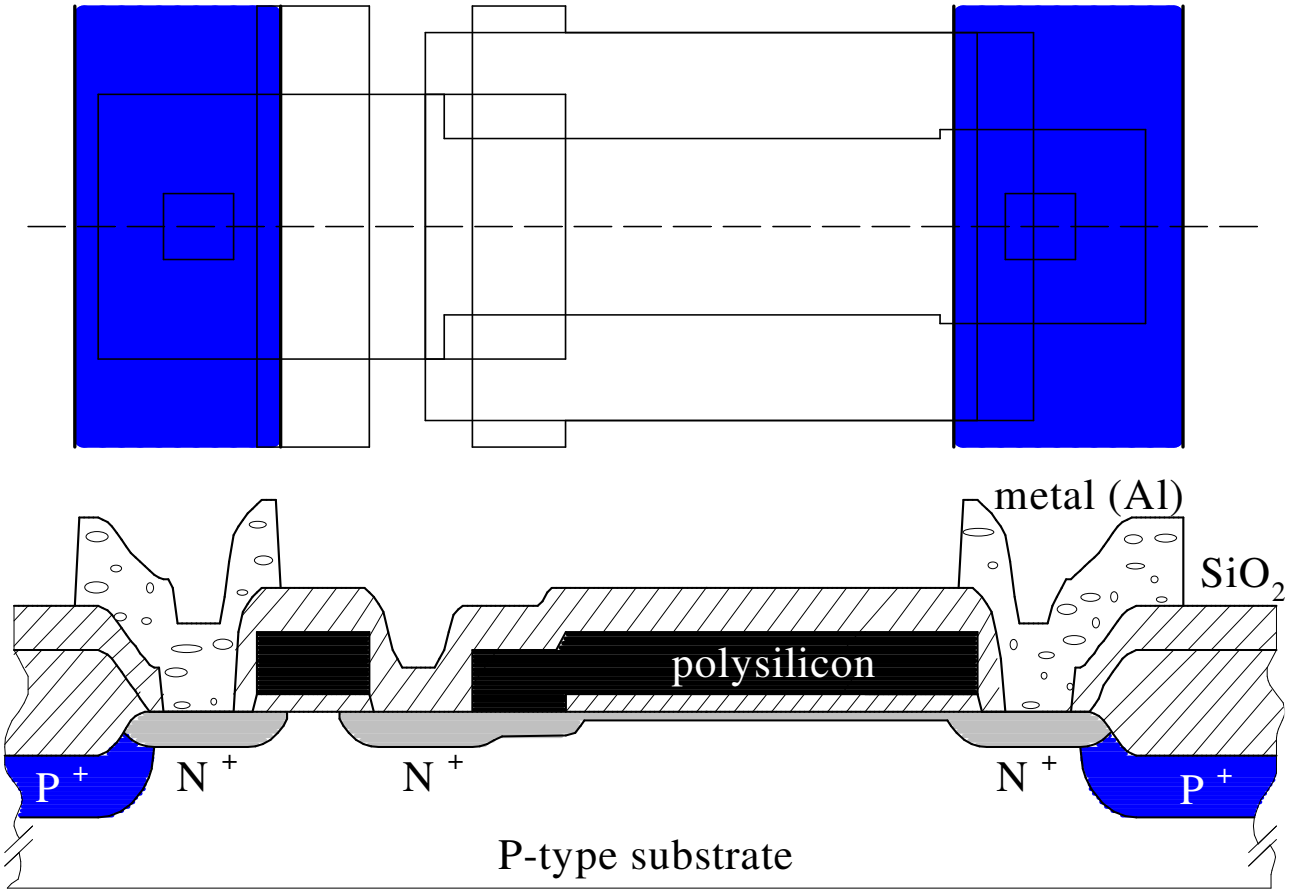
(a)


GND
metal (Al)
V_+
SiO_2
Input
Output
built-in channel
P^+
N^+ source
N^+ drain/source
N^+ drain
P^+
P-type substrate (bulk)

(b)


Input
Output
V_+

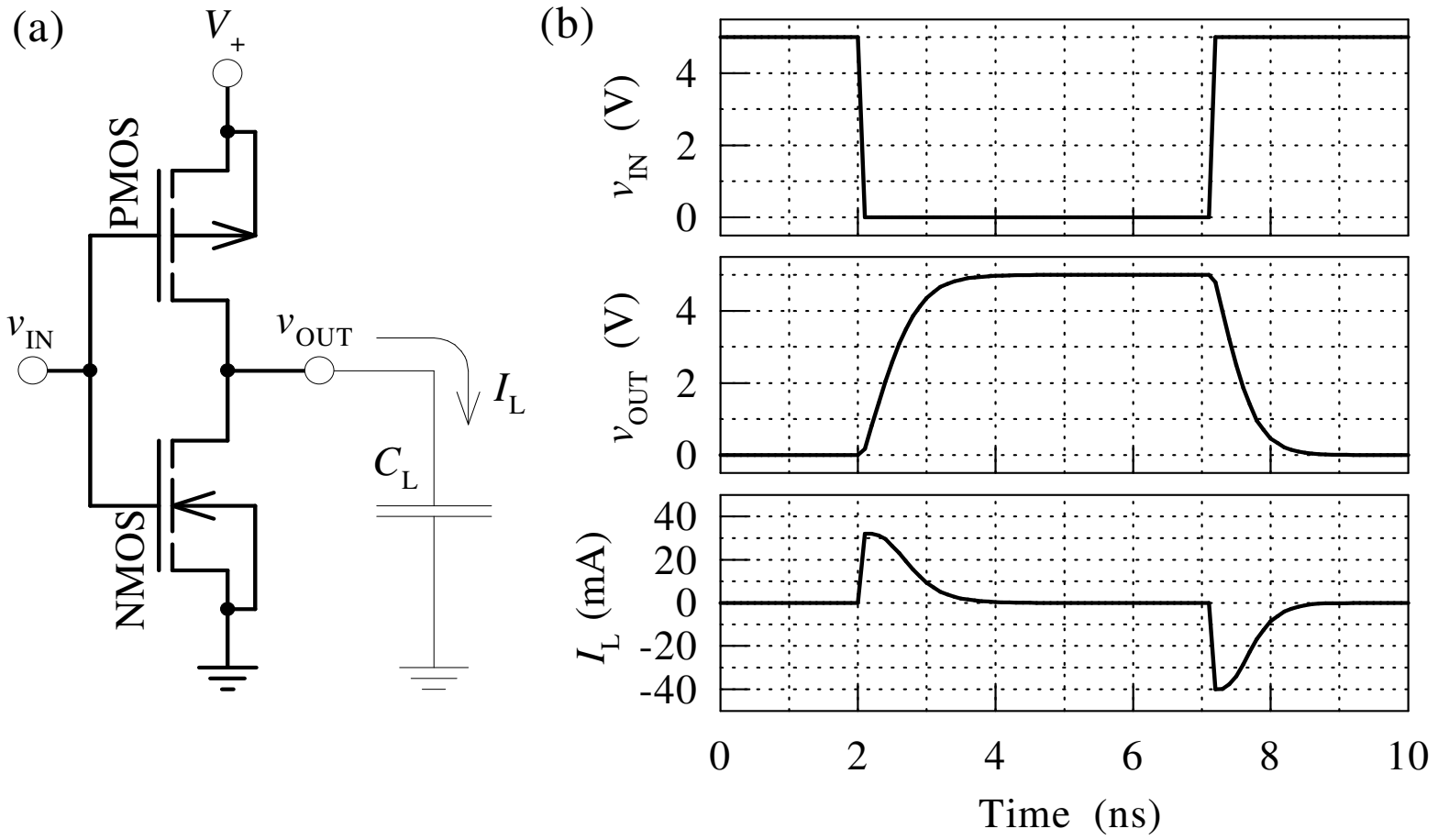
(c)

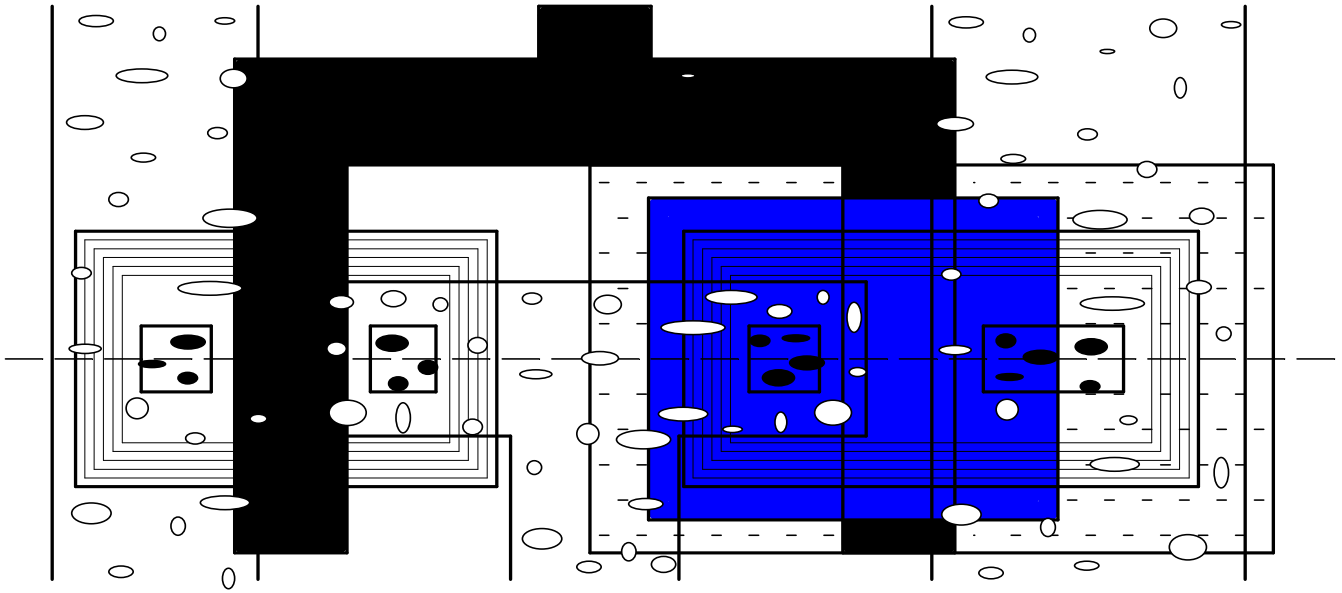


(i)

- aluminum deposition
- Photolithography VI: metallization patterning

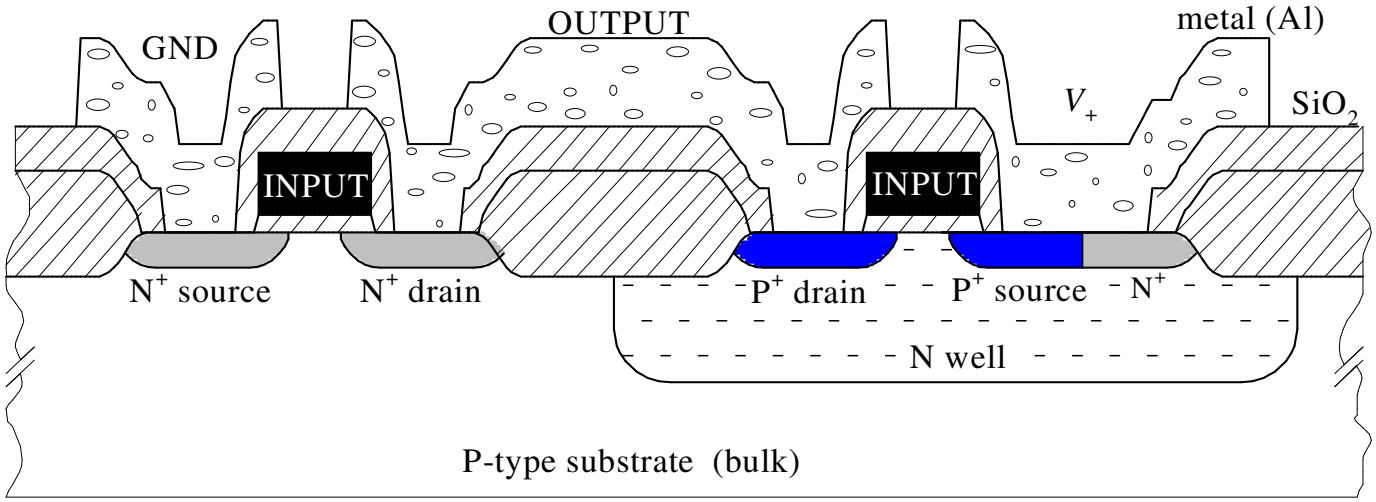
Complementary MOS (CMOS) Transistors



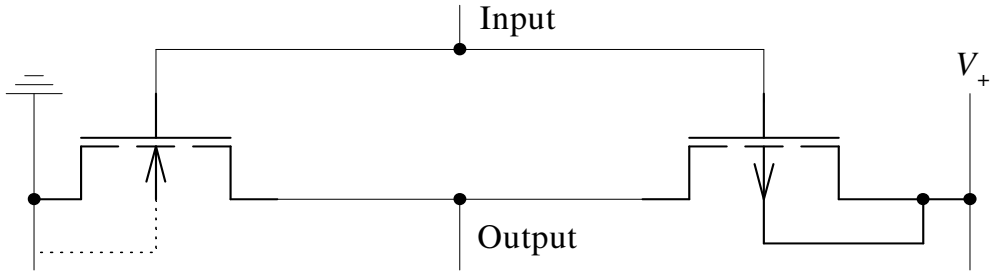


N well
Active areas
Polysilicon
$P^+(N^+)$ doping
Contacts
Metal

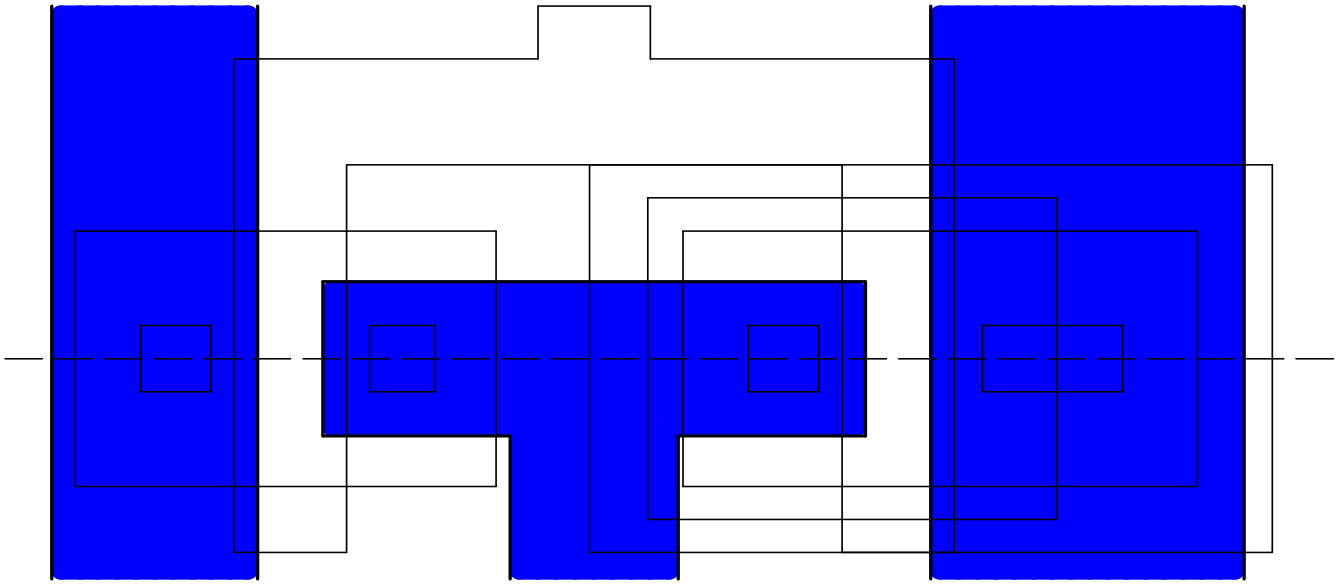
(a)

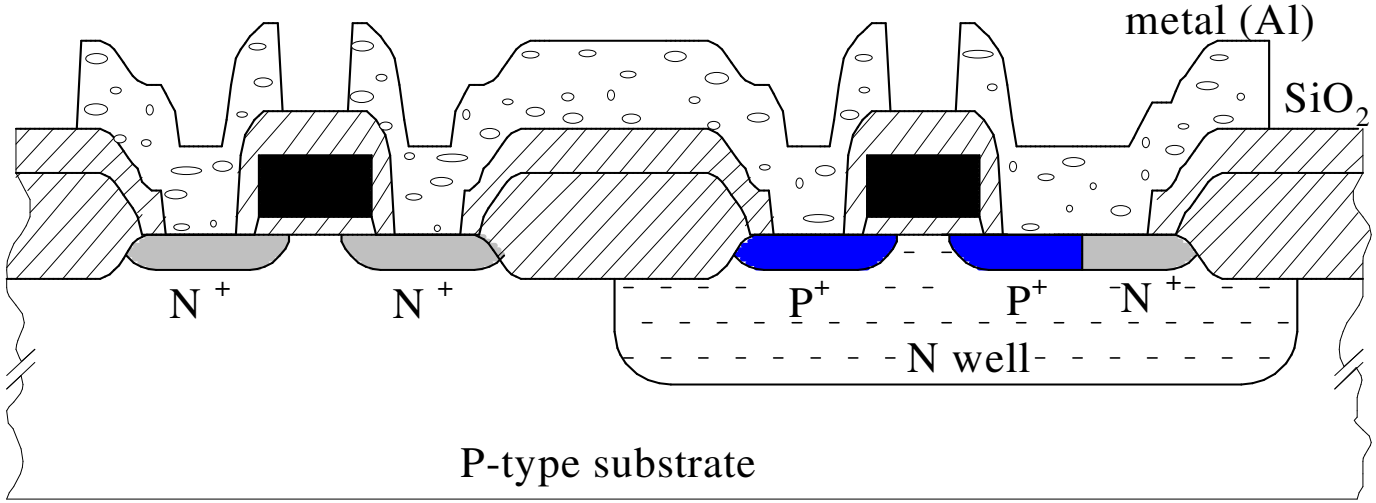


(b)



(c)

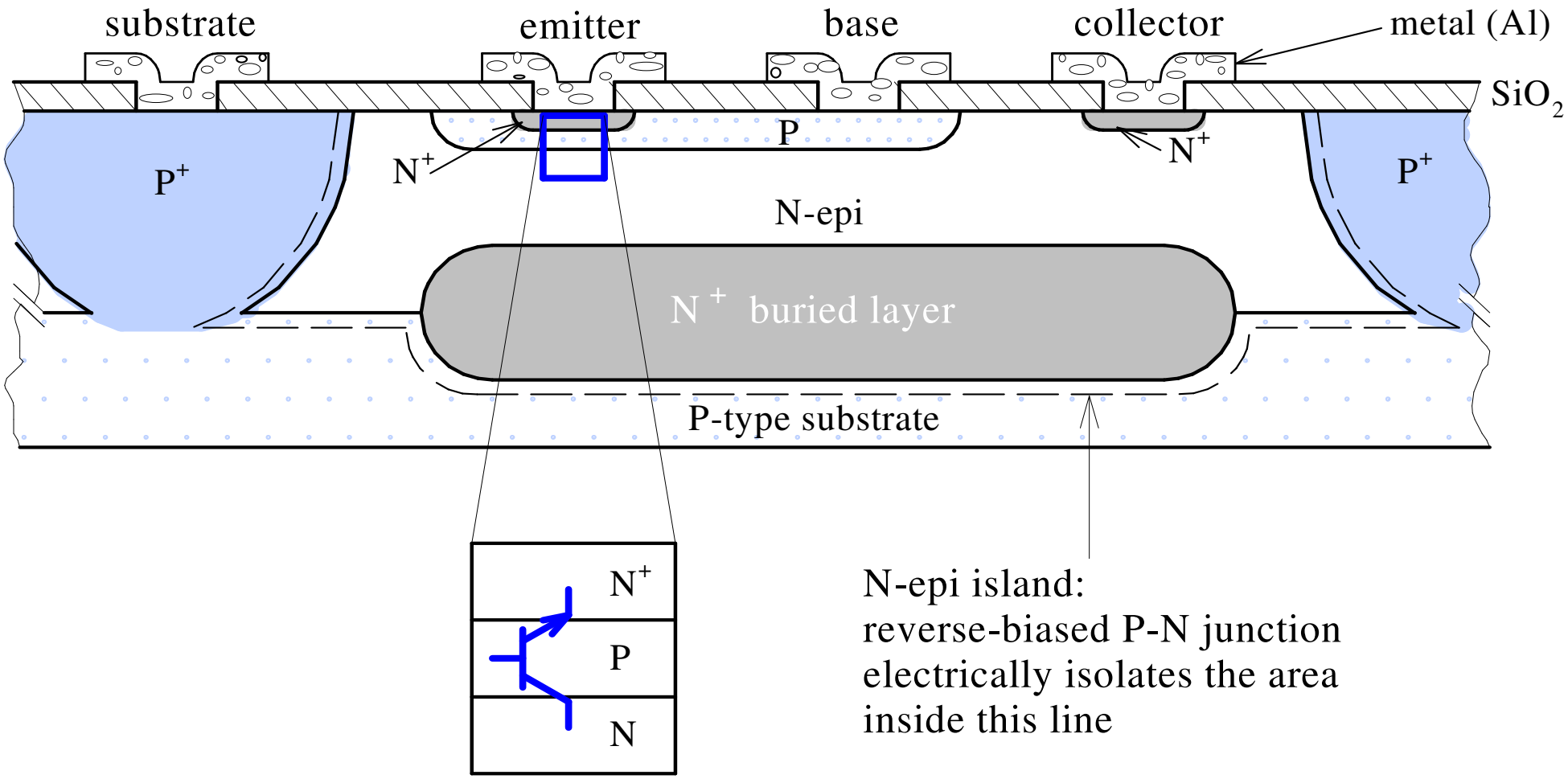


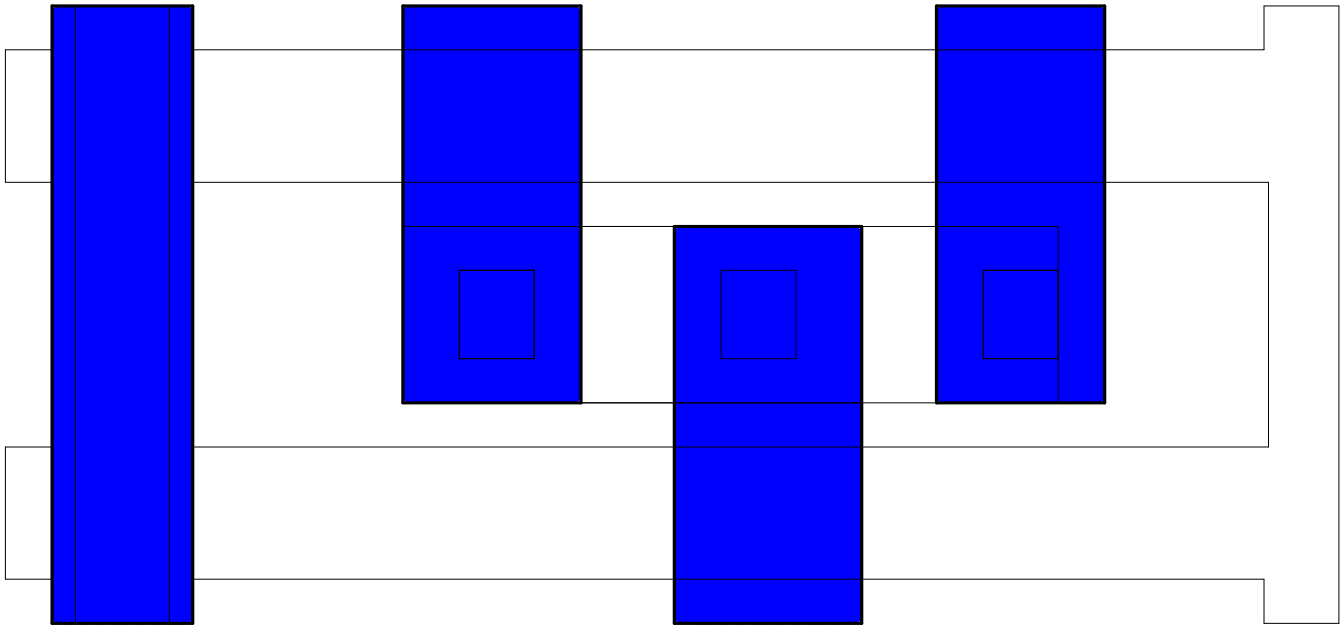


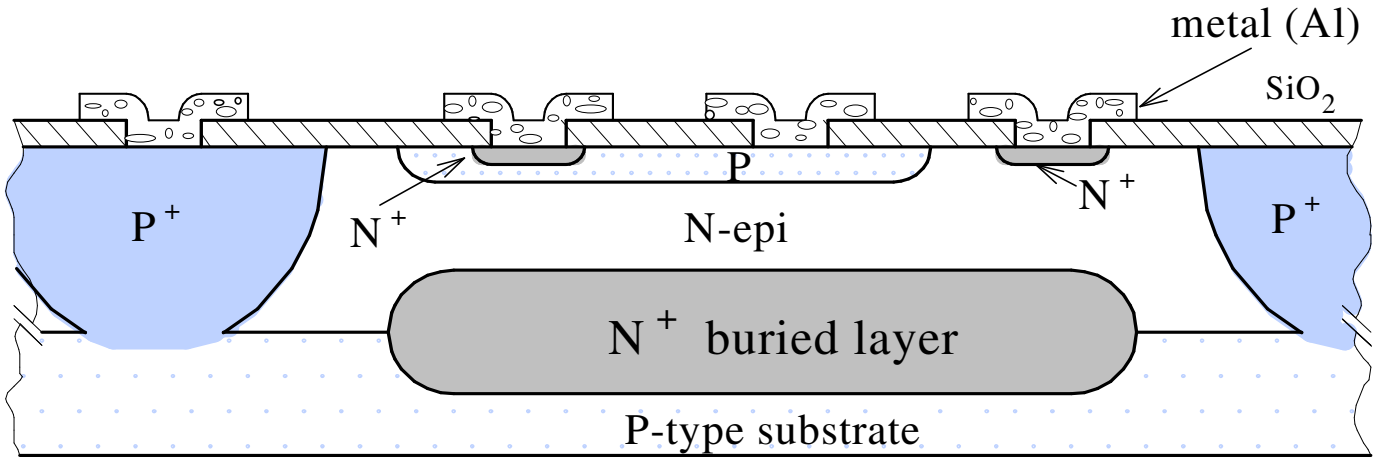
(i)

- aluminum deposition
- Photolithography VII: metallization patterning

Bipolar NPN Transistor

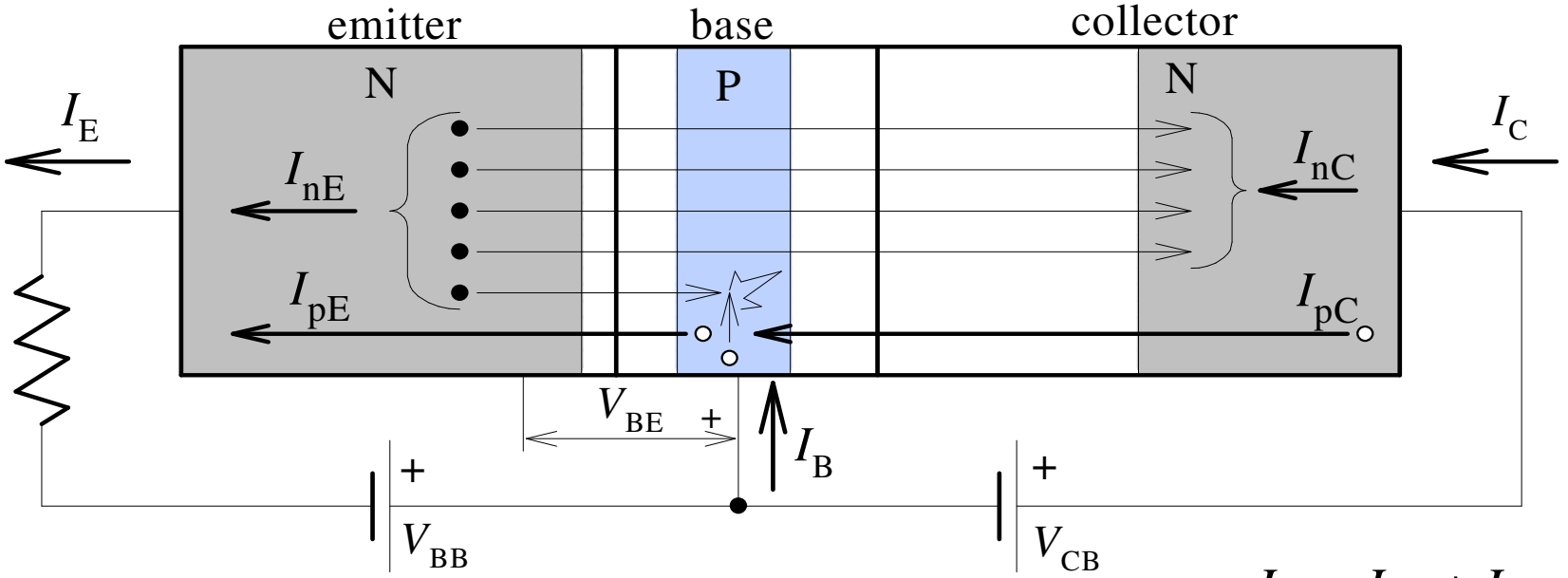






(g)

- aluminum deposition
- Photolithography VI: metallization patterning



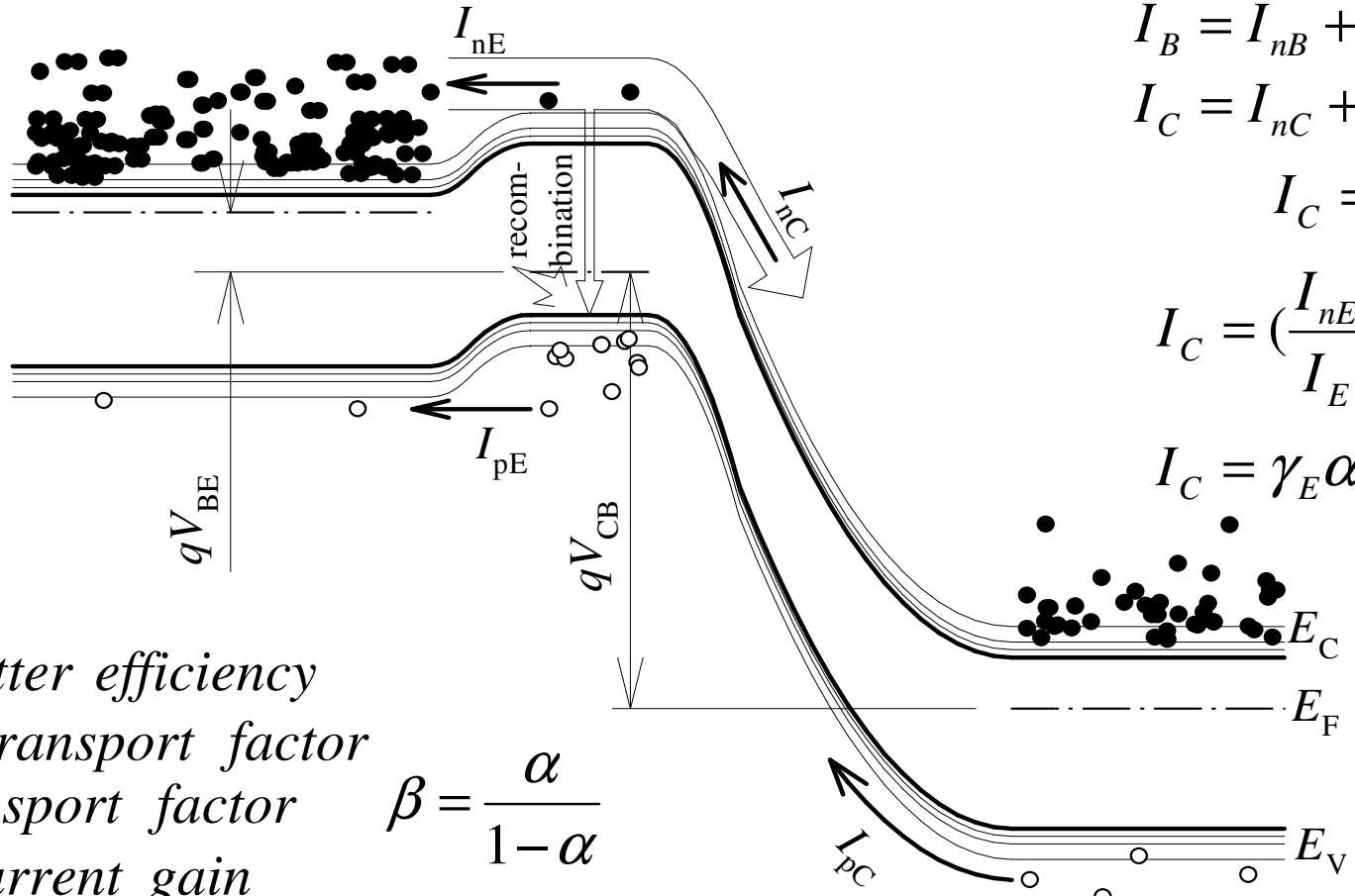
(a)

$$I_E = I_{nE} + I_{pE} \qquad I_{nE} = I_{nB} + I_{nC}$$
$$I_B = I_{nB} + I_{pB} \qquad I_{pE} = I_{pB} + I_{pC}$$
$$I_C = I_{nC} + I_{pC} \qquad I_E = I_B + I_C$$

$$I_C = I_{nE} - I_{nB} + I_{pC}$$

$$I_C = \left(\frac{I_{nE}}{I_E} \times \frac{I_{nE} - I_{nB}}{I_{nE}} + \frac{I_{pC}}{I_E}\right) I_E \qquad (I_{pC} \to 0)$$

$$I_C = \gamma_E \alpha_T I_E = \alpha I_E = \frac{\alpha}{1-\alpha} I_B$$



(b)

γ_E – *emitter efficiency*

α_T – *base transport factor*

α – *transport factor*

β – *current gain*

$$\beta = \frac{\alpha}{1-\alpha}$$

Emitter Efficiency and Base Transport Factor

$$I_{nE} = qS\frac{L_n n_{B0}}{\tau_n}\left(e^{\frac{qV_{BE}}{KT}} - 1\right) = qS\frac{D_n n_i^2}{w_B N_{aB}}\left(e^{\frac{qV_{BE}}{KT}} - 1\right)$$

$$I_{pE} = qS\frac{L_p p_{E0}}{\tau_p}\left(e^{\frac{qV_{BE}}{KT}} - 1\right) = qS\frac{D_p n_i^2}{L_p N_{dE}}\left(e^{\frac{qV_{BE}}{KT}} - 1\right)$$

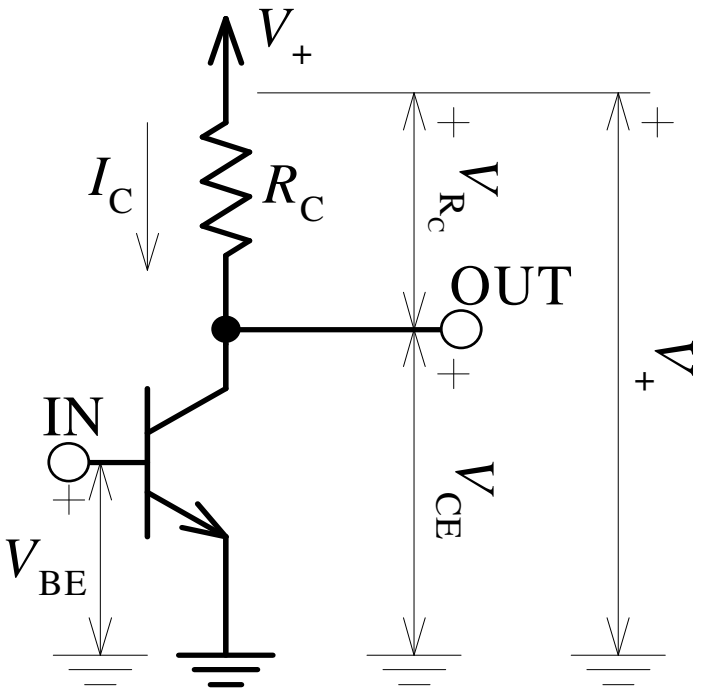
$$\gamma_E = \frac{1}{1 + \frac{D_p w_B N_{aB}}{D_n L_p N_{dE}}} \approx 1 - \frac{D_p w_B N_{aB}}{D_n L_p N_{dE}}$$

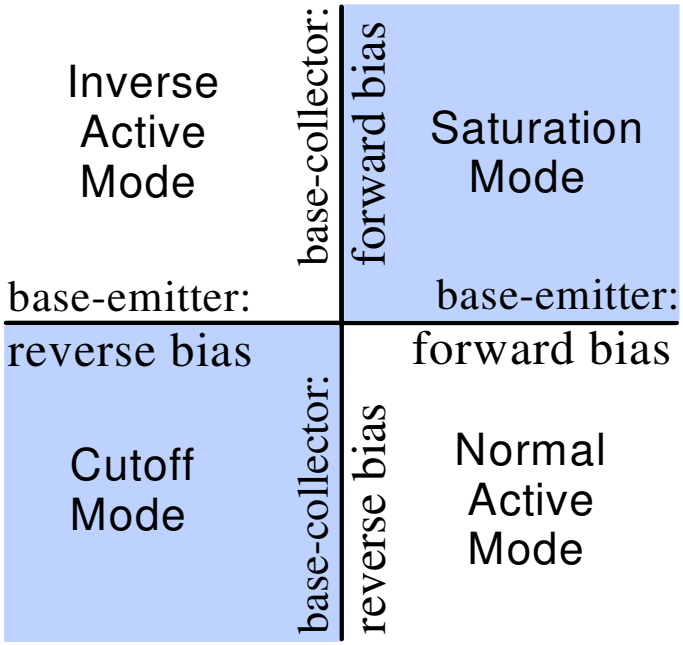
$$I_{nE} = qS\frac{D_n n_i^2}{w_B N_{aB}}\left(e^{\frac{qV_{BE}}{KT}} - 1\right) = \frac{\Delta Q_{nB}}{t_r}$$

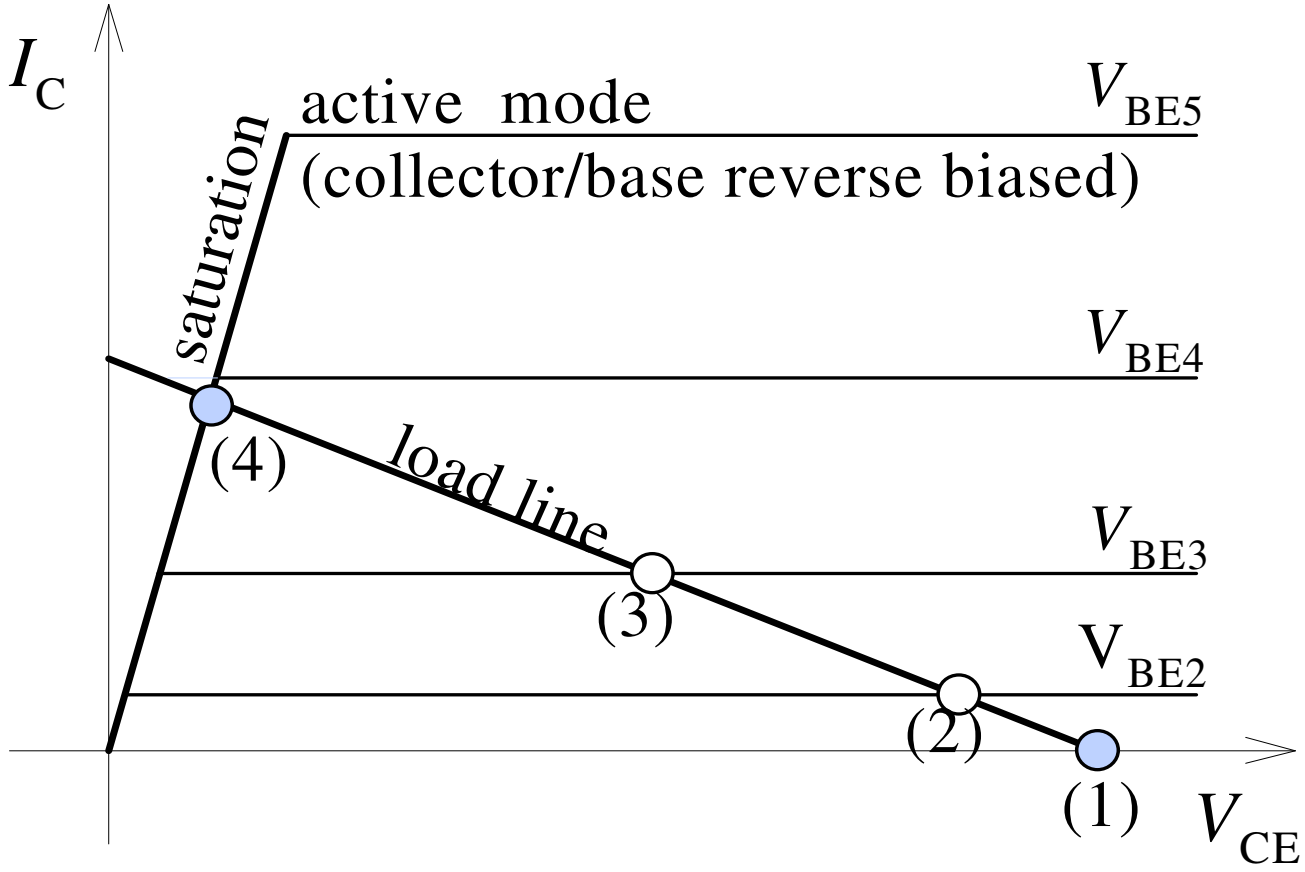
$$\Delta Q_{nB} = qS\frac{n_i^2}{N_{aB}}\left(e^{\frac{qV_{BE}}{KT}} - 1\right)\frac{w_B}{2} \Rightarrow t_r = \frac{w_B^2}{2D_n}$$

$$\alpha_T = 1 - \frac{t_r}{\tau_n} = 1 - \frac{w_B^2}{2D_n\tau_n} = 1 - \frac{w_B^2}{2L_n^2}$$

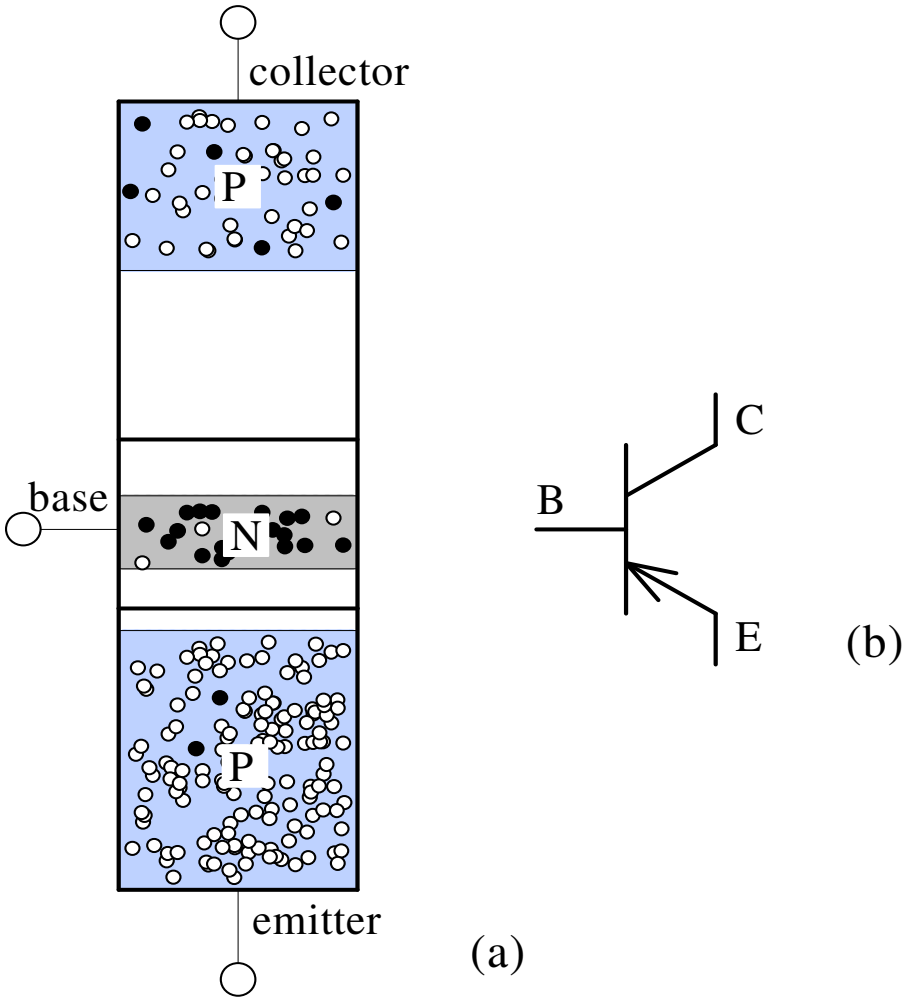
$$I_{nB} = \frac{\Delta Q_{nB}}{\tau_n}$$

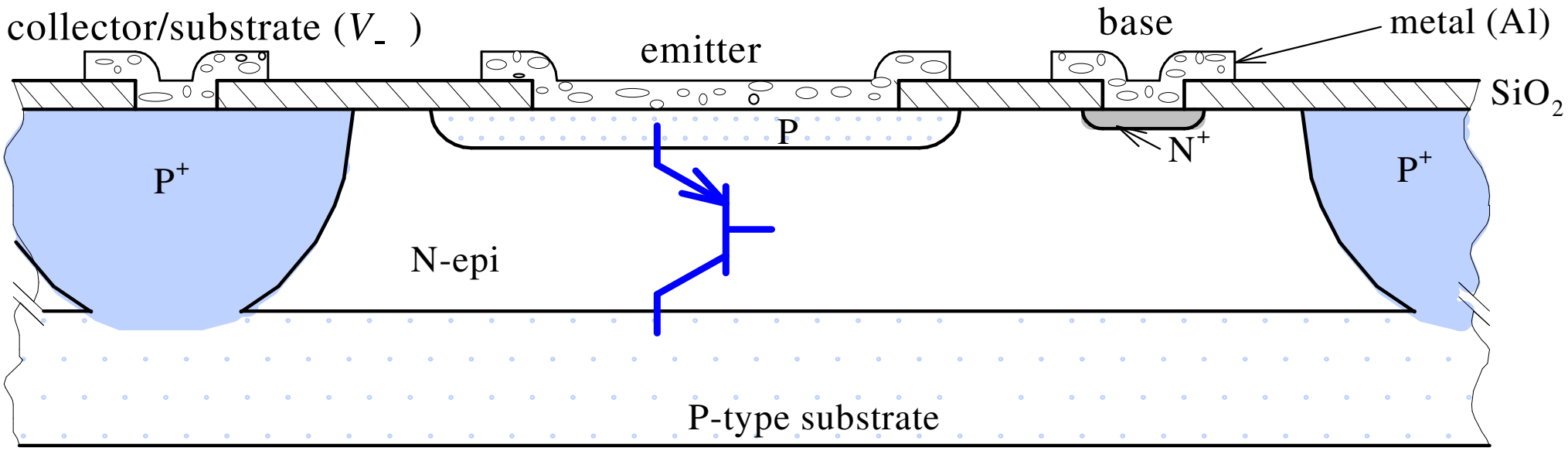

V_+
I_C
R_C
V_{R_C}
OUT
IN
V_{CE}
V_+
V_{BE}

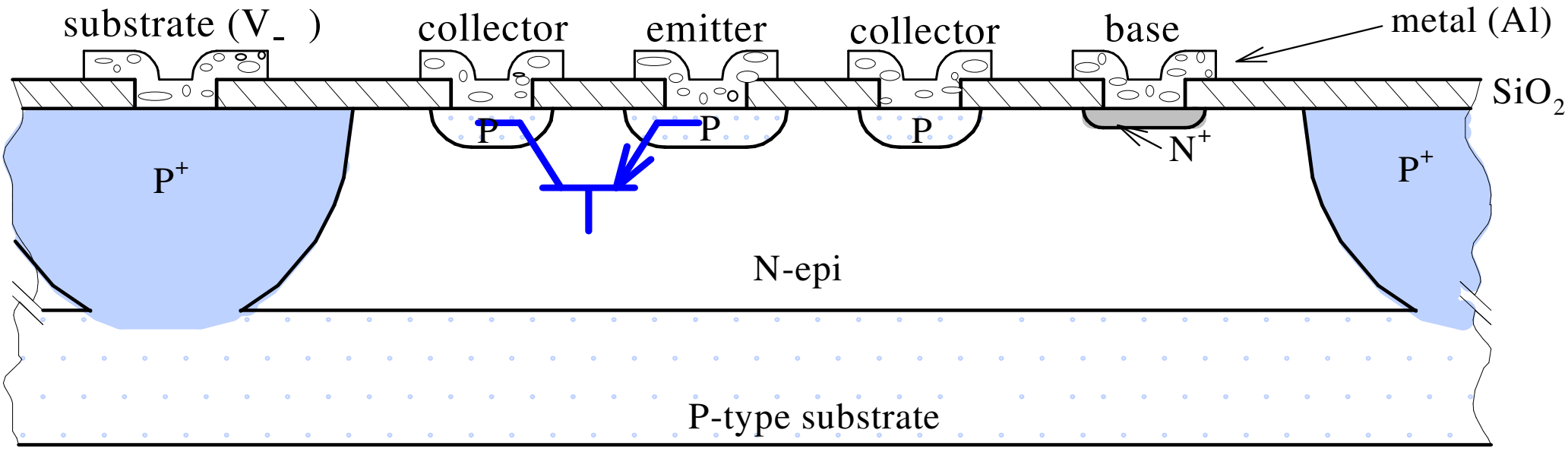

Inverse Active Mode
base-collector: forward bias
Saturation Mode
base-emitter: reverse bias
base-emitter: forward bias
Cutoff Mode
base-collector: reverse bias
Normal Active Mode


I_C
active mode
(collector/base reverse biased)
saturation
V_{BE5}
V_{BE4}
V_{BE3}
V_{BE2}
(4)
load line
(3)
(2)
(1)
V_{CE}

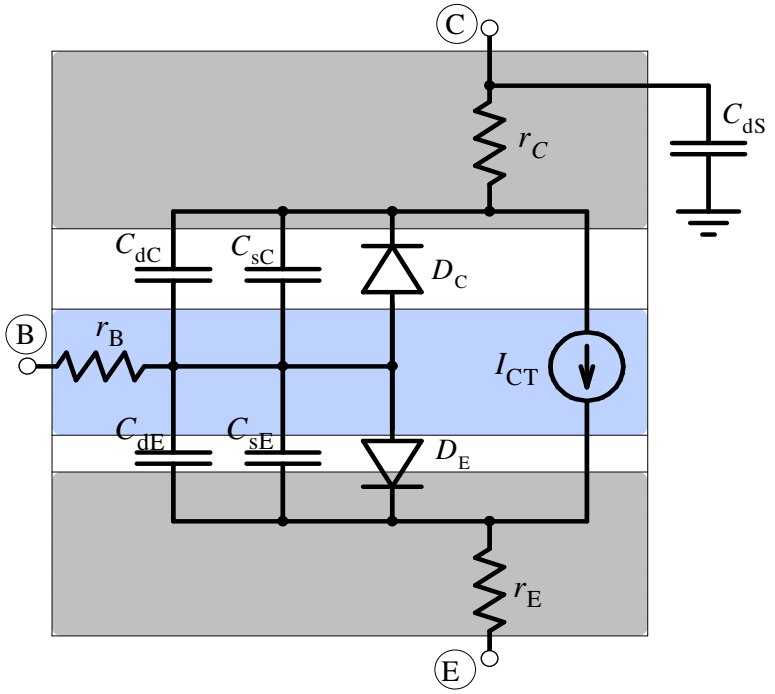
Bipolar PNP Transistor

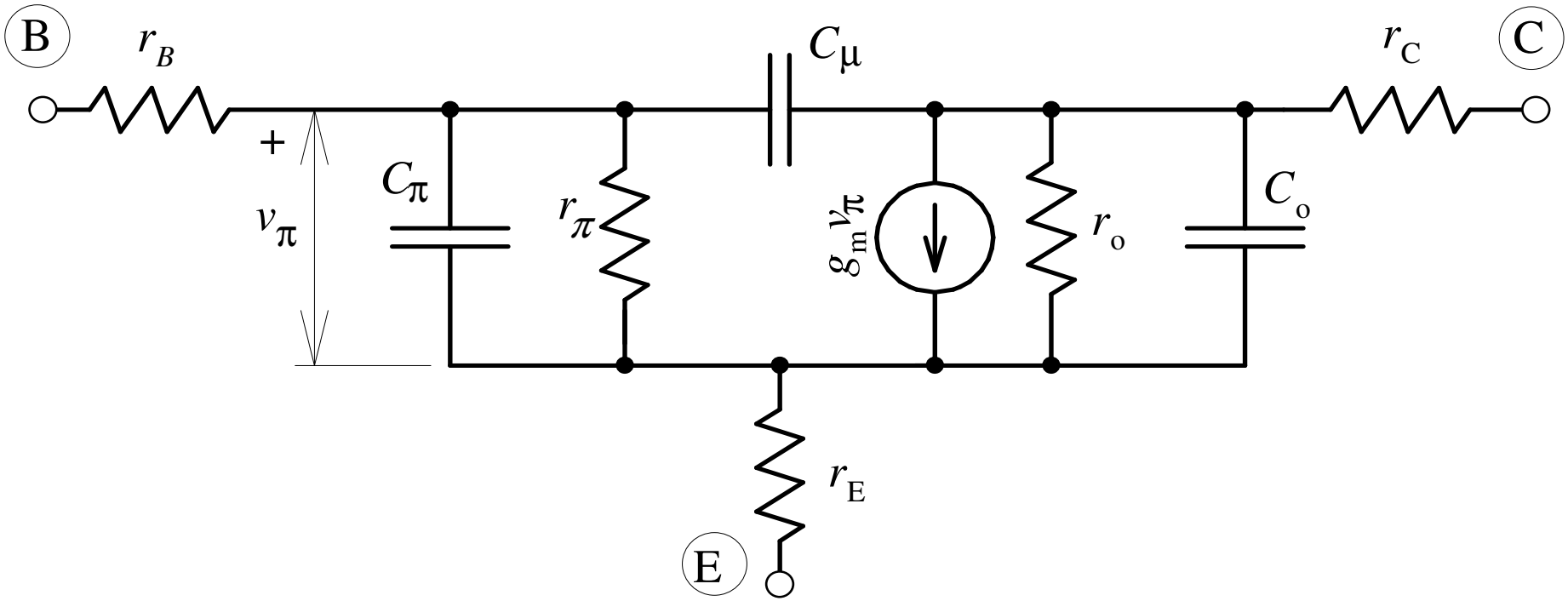



collector/substrate (V_-)
emitter
base
metal (Al)
SiO_2
P
P^+
N^+
P^+
N-epi
P-type substrate

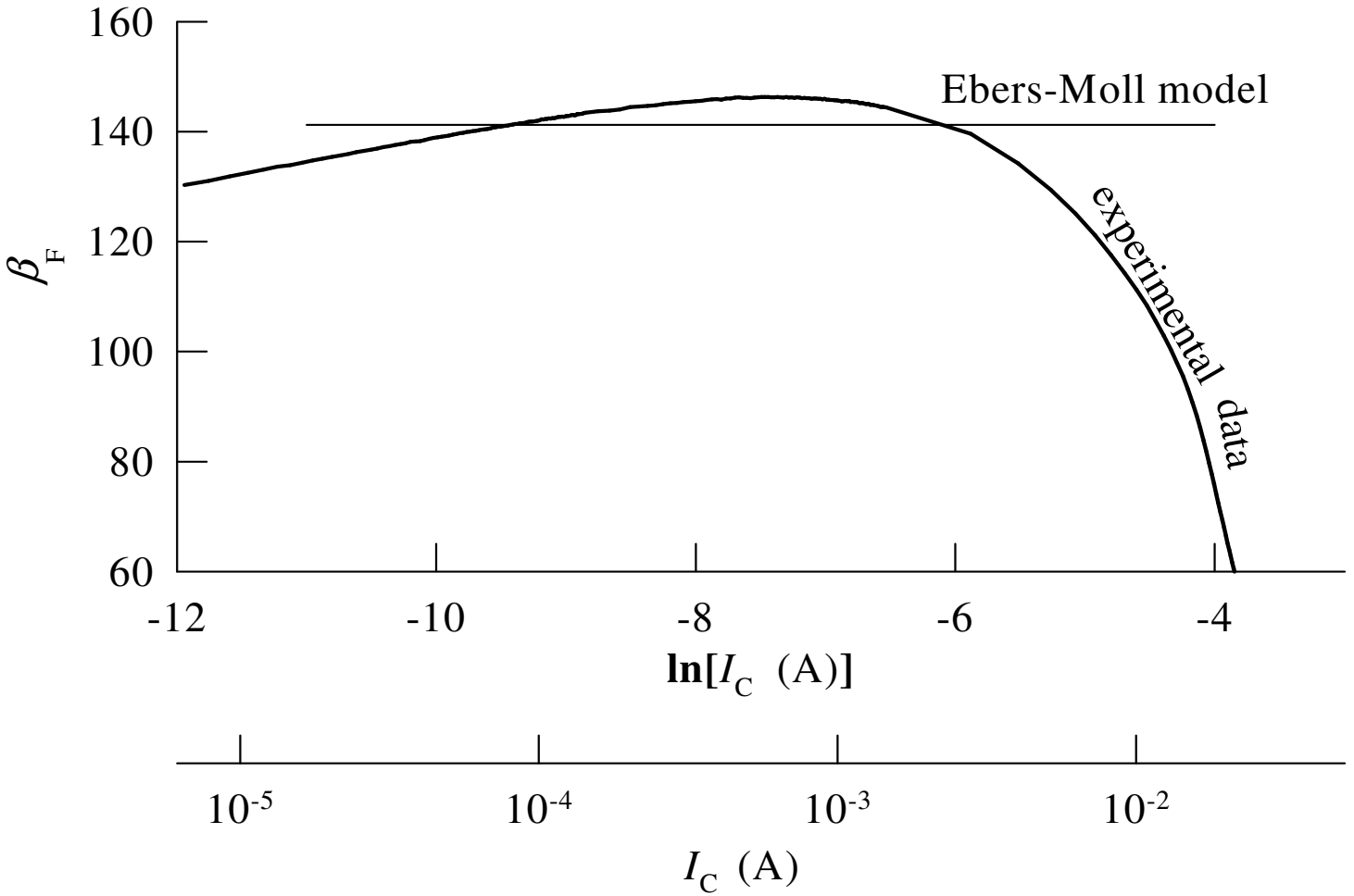

substrate (V_-)
collector
emitter
collector
base
metal (Al)
SiO_2
P
P
P
N^+
P^+
P^+
N-epi
P-type substrate

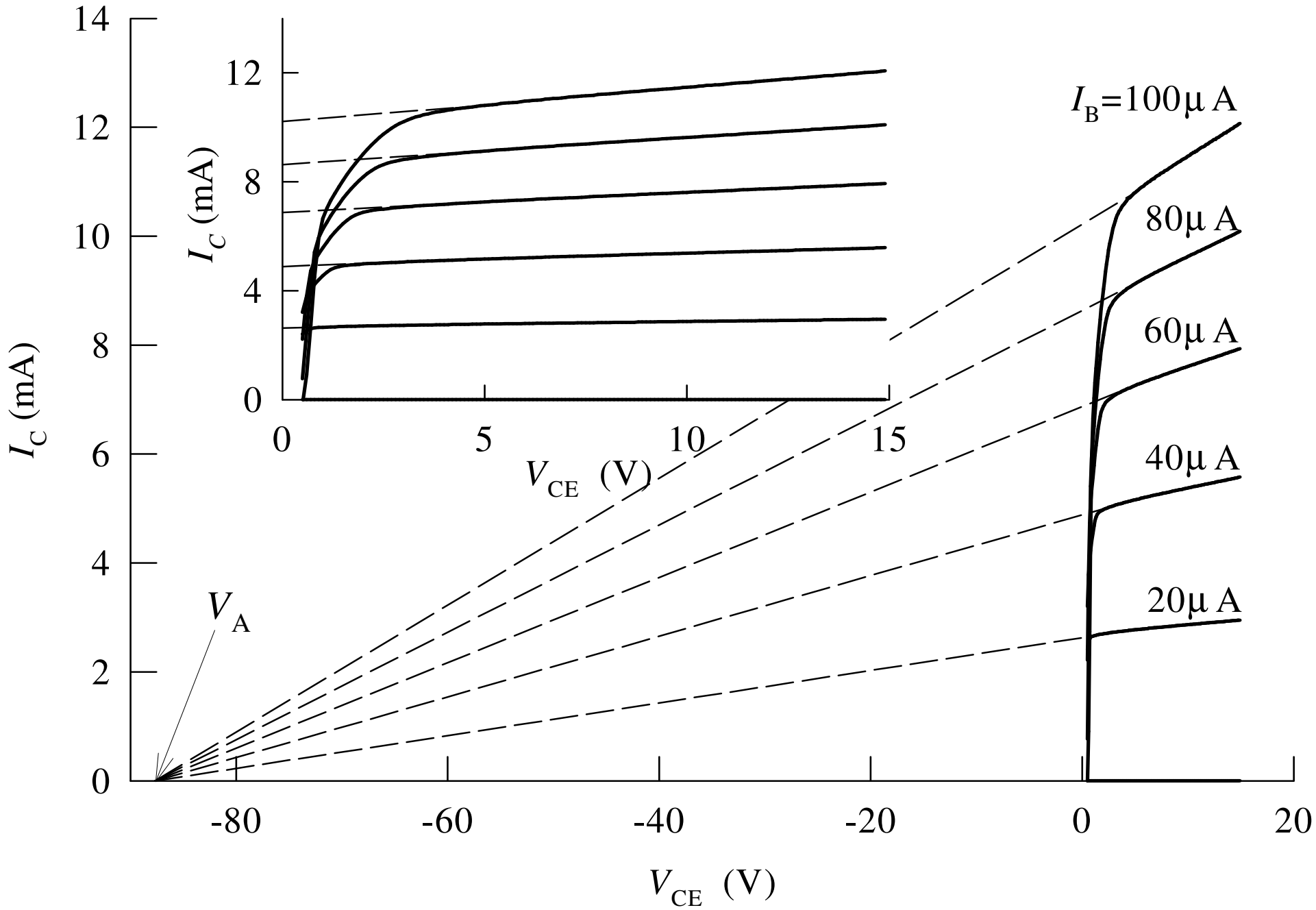
Electrical Model



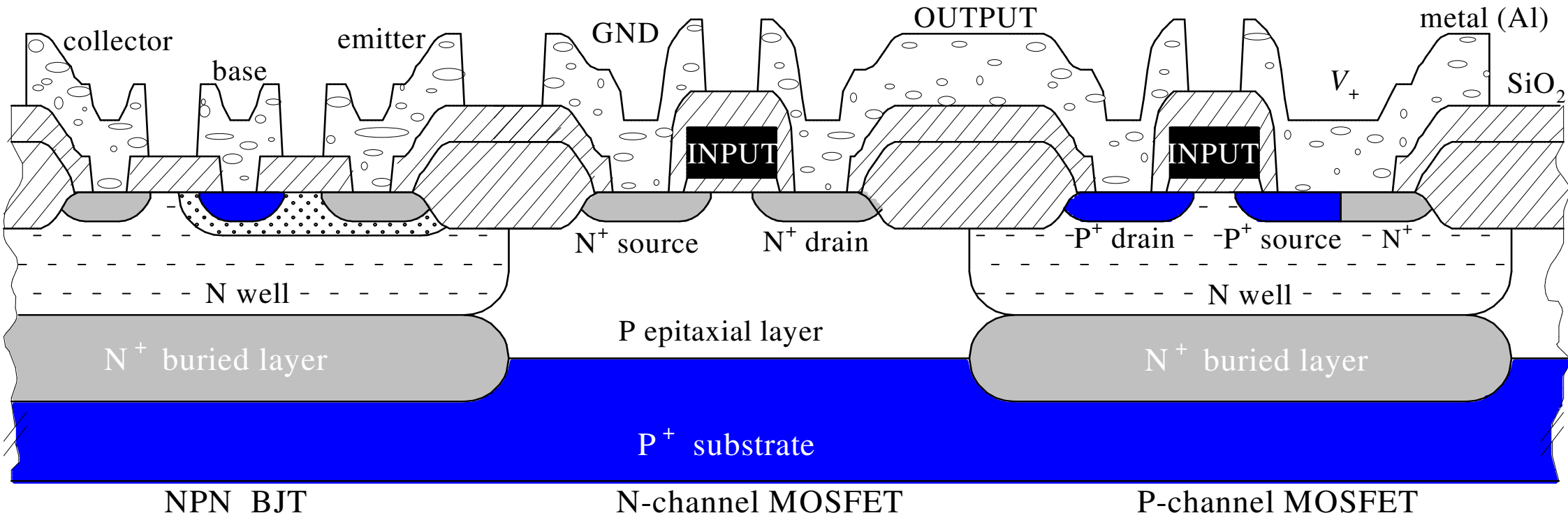


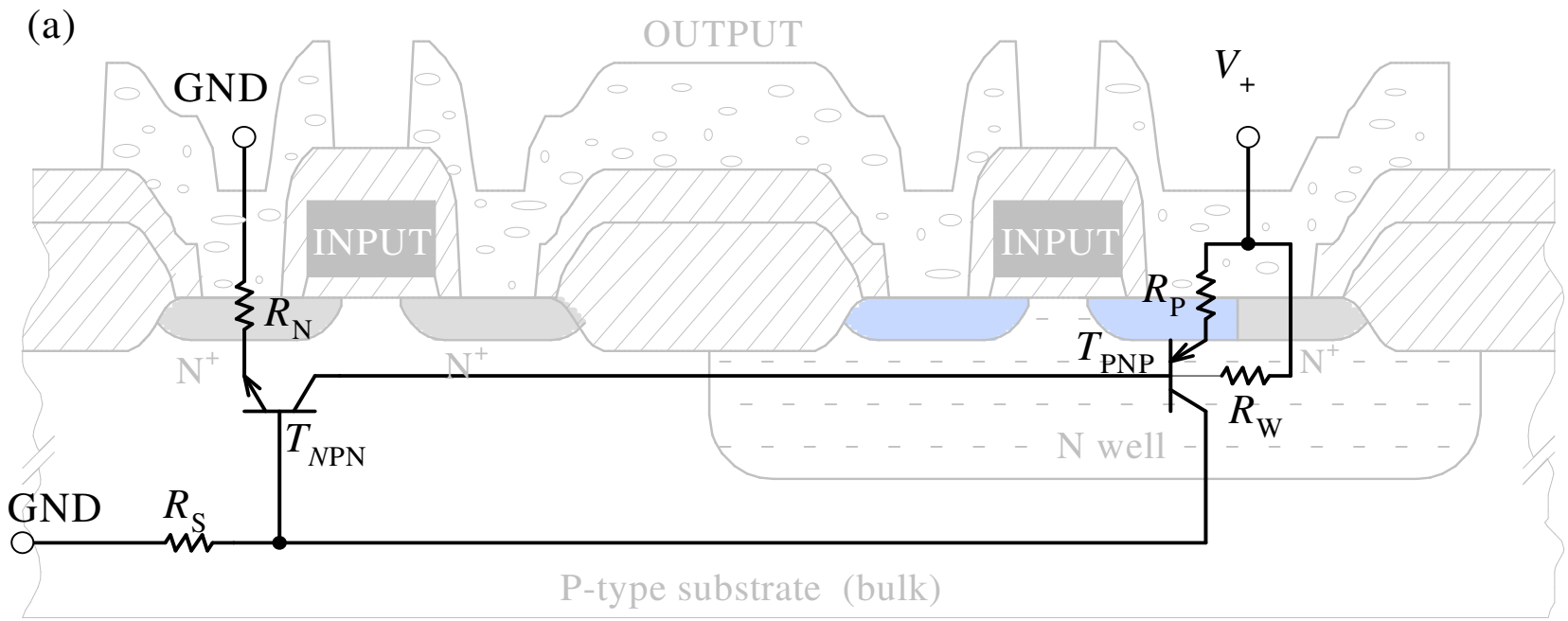
Current Gain

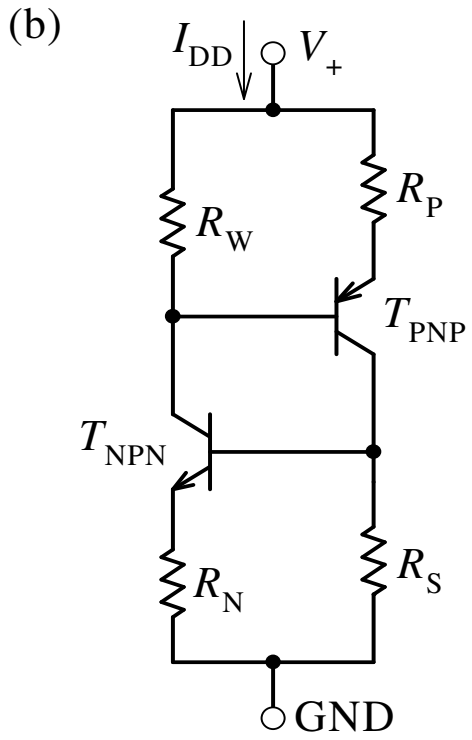


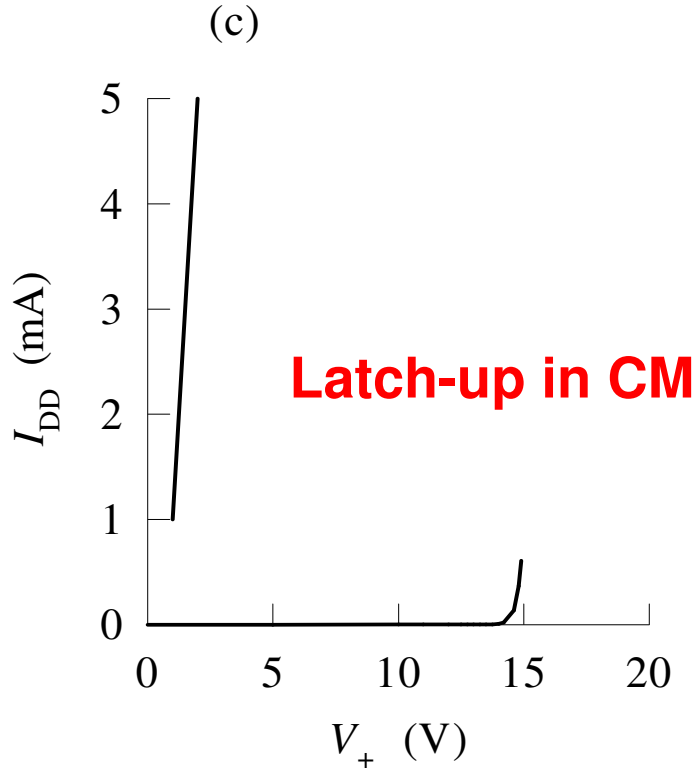

14
12
10
8
6
4
2
0
I_C (mA)
-80
-60
-40
-20
0
20
V_{CE} (V)
V_A
I_B=100μ A
80μ A
60μ A
40μ A
20μ A
12
8
4
0
I_C (mA)
0
5
10
15
V_{CE} (V)

Bipolar Transistor in CMOS Technology





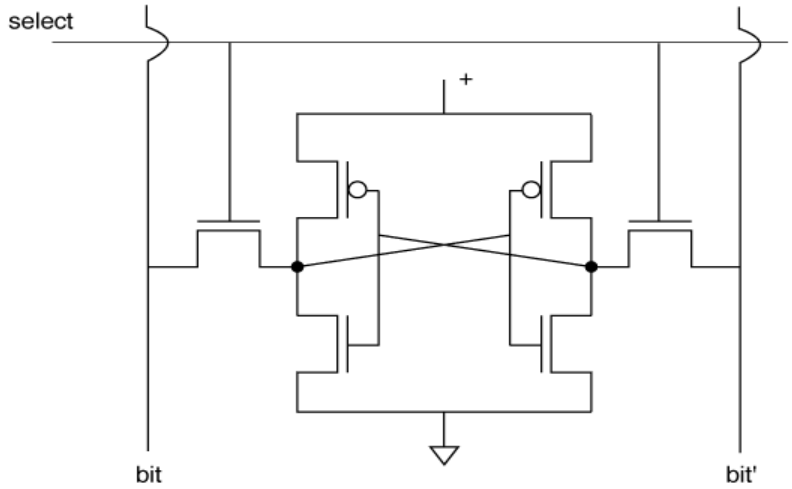


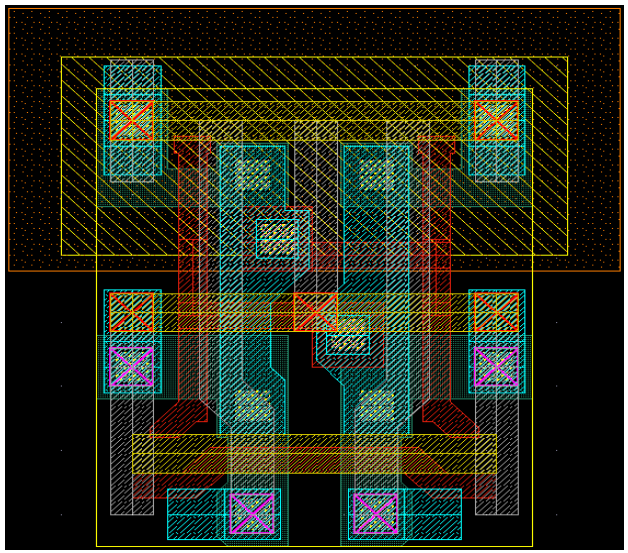


Latch-up in CMOS Technology

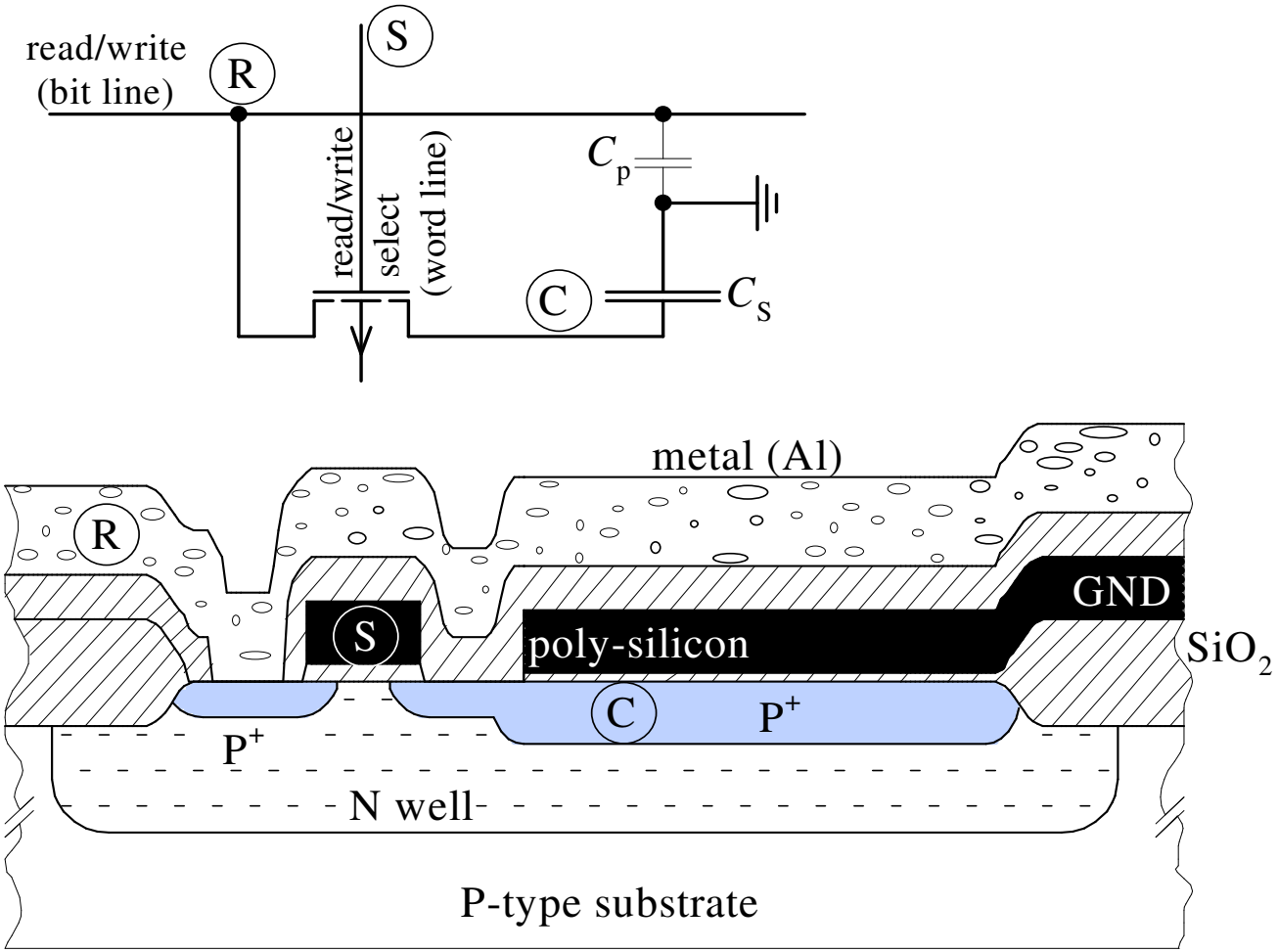
Static Random Access Memory

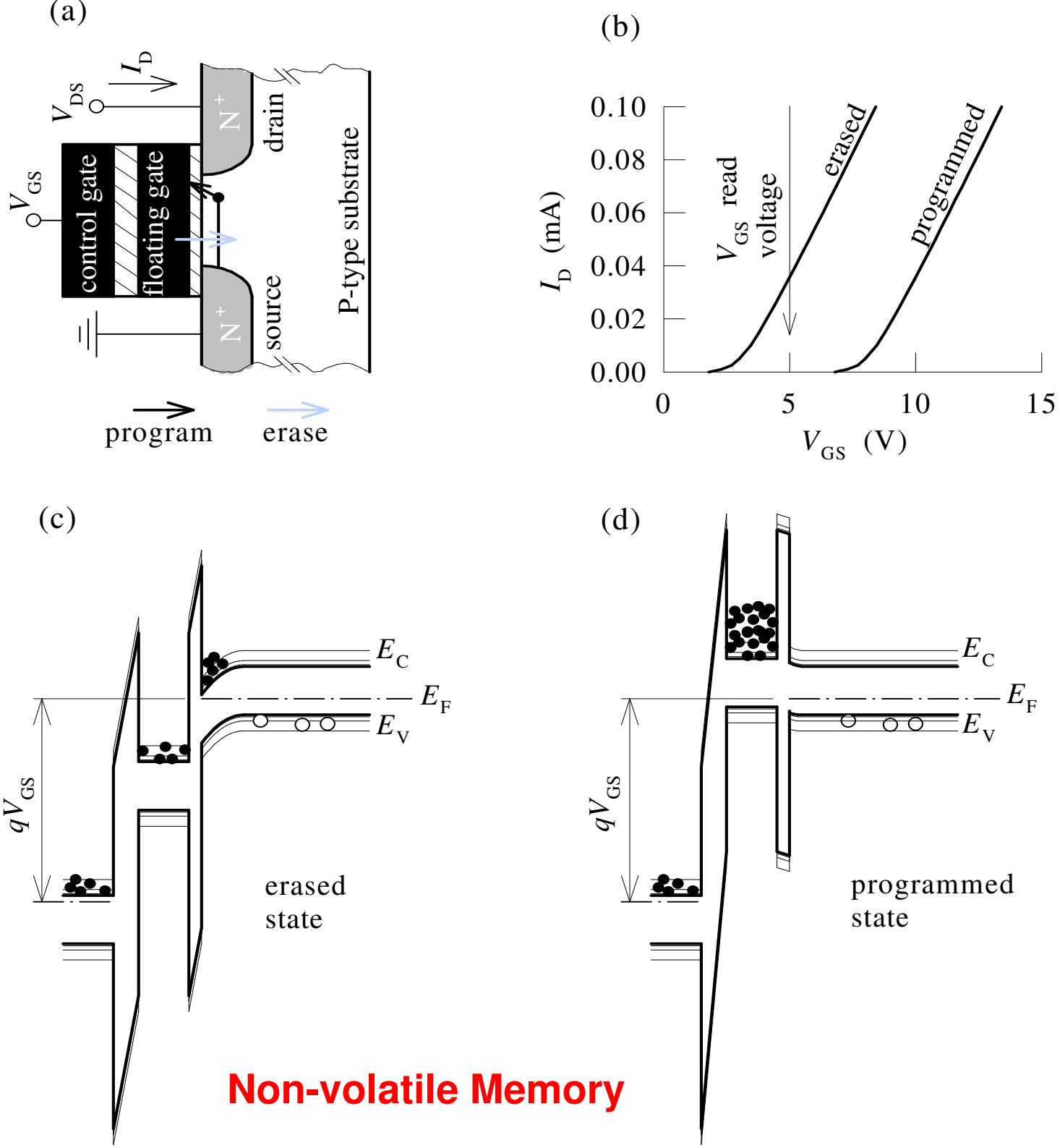
- Value is stored symmetrically
  - Both true and complement are stored on cross-coupled transistors
- SRAM retains value as long as power is applied to circuit
- Read
  - Precharge bit and bit' high
  - Set select line high from row decoder
  - One bit line will be pulled down
- Write
  - Set bit/bit' to desired (complementary) values
  - Set select line high
  - Drive on bit lines will flip state if necessary





Dynamic Random Access Memory




(a)
I_D
V_{DS}
N^+
drain
V_{GS}
control gate
floating gate
P-type substrate
N^+
source
program
erase
(b)
0.10
0.08
0.06
0.04
0.02
0.00
I_D (mA)
V_{GS} read voltage
erased
programmed
0
5
10
15
V_{GS} (V)
(c)
E_C
E_F
E_V
qV_{GS}
erased state
(d)
E_C
E_F
E_V
qV_{GS}
programmed state
Non-volatile Memory