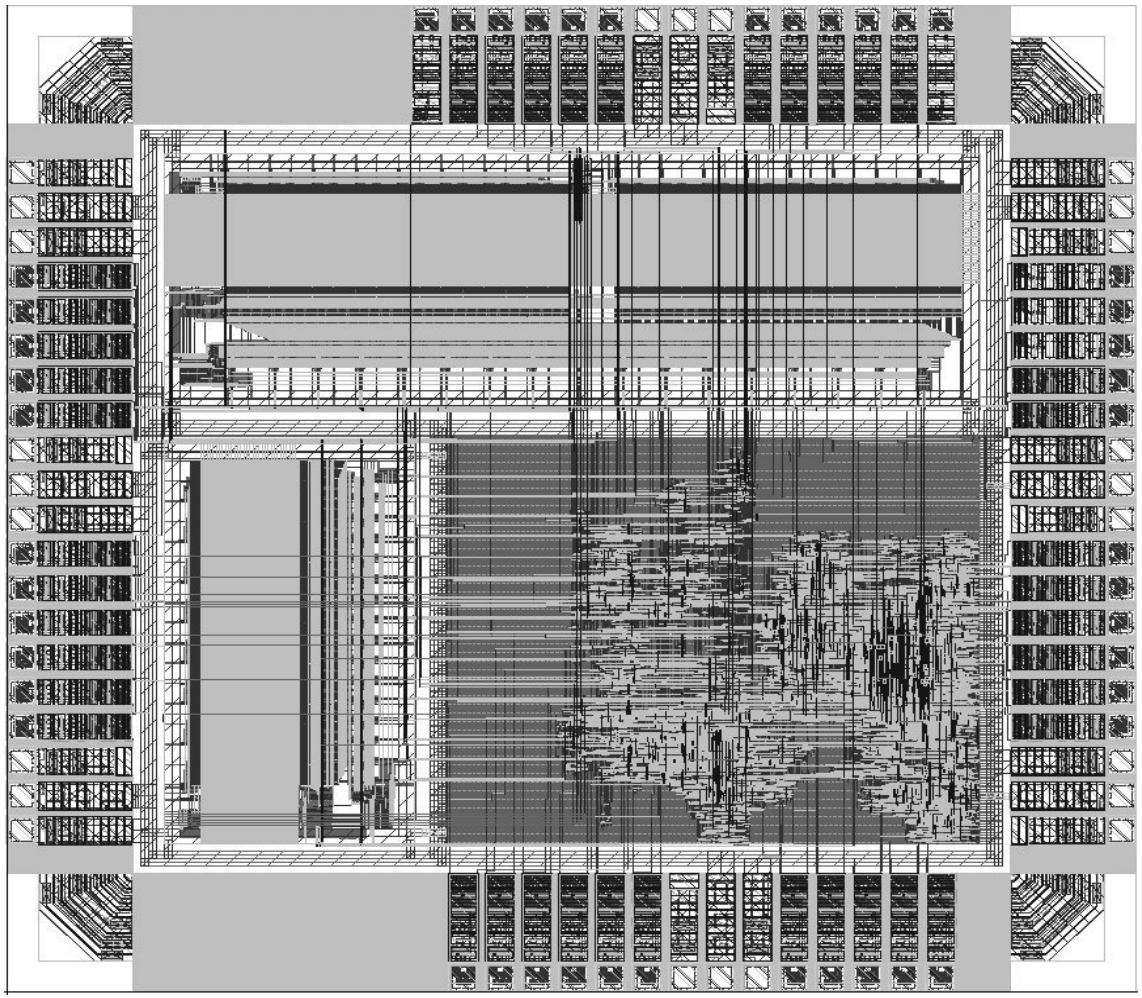
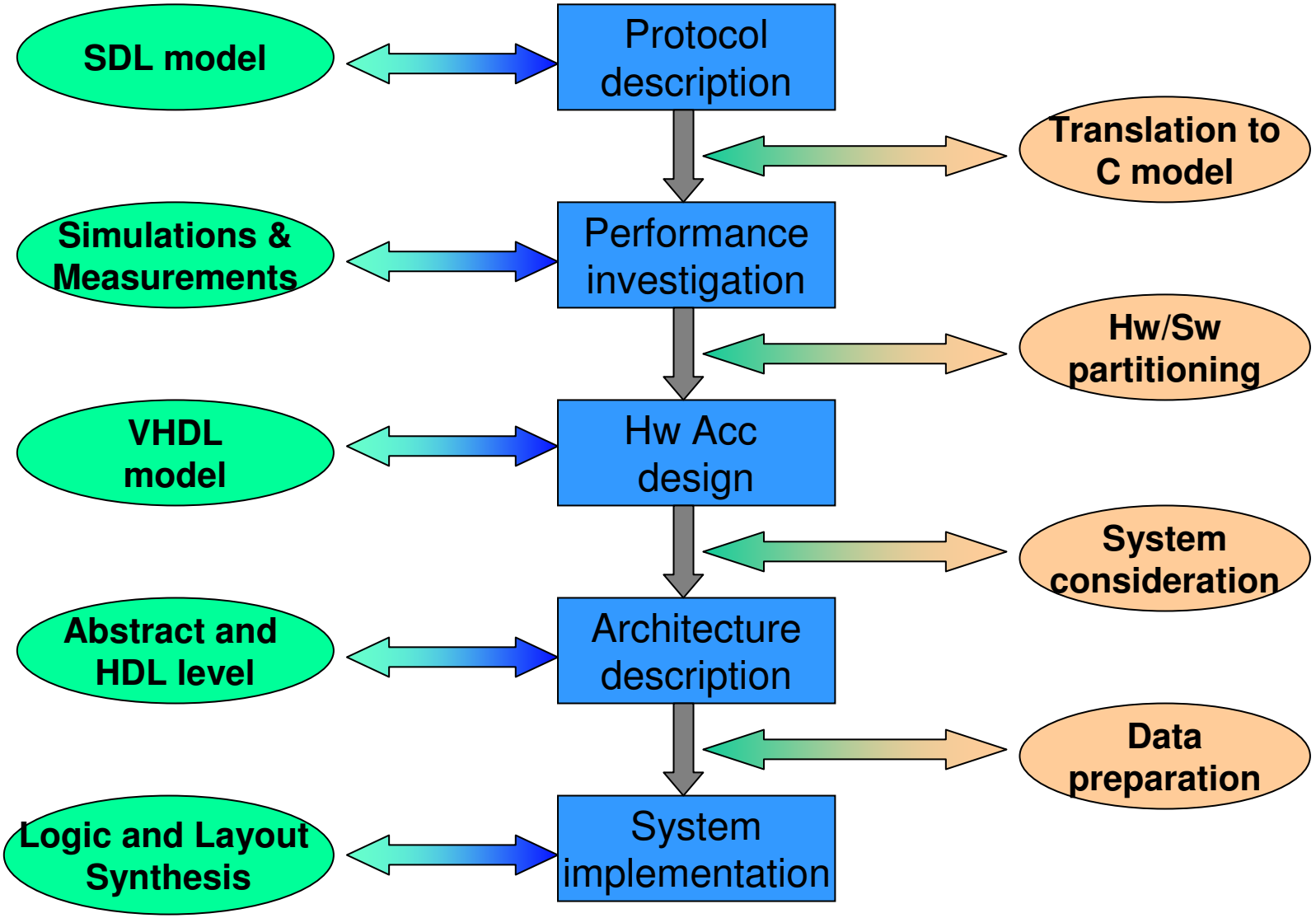
TANDEM SOC Features



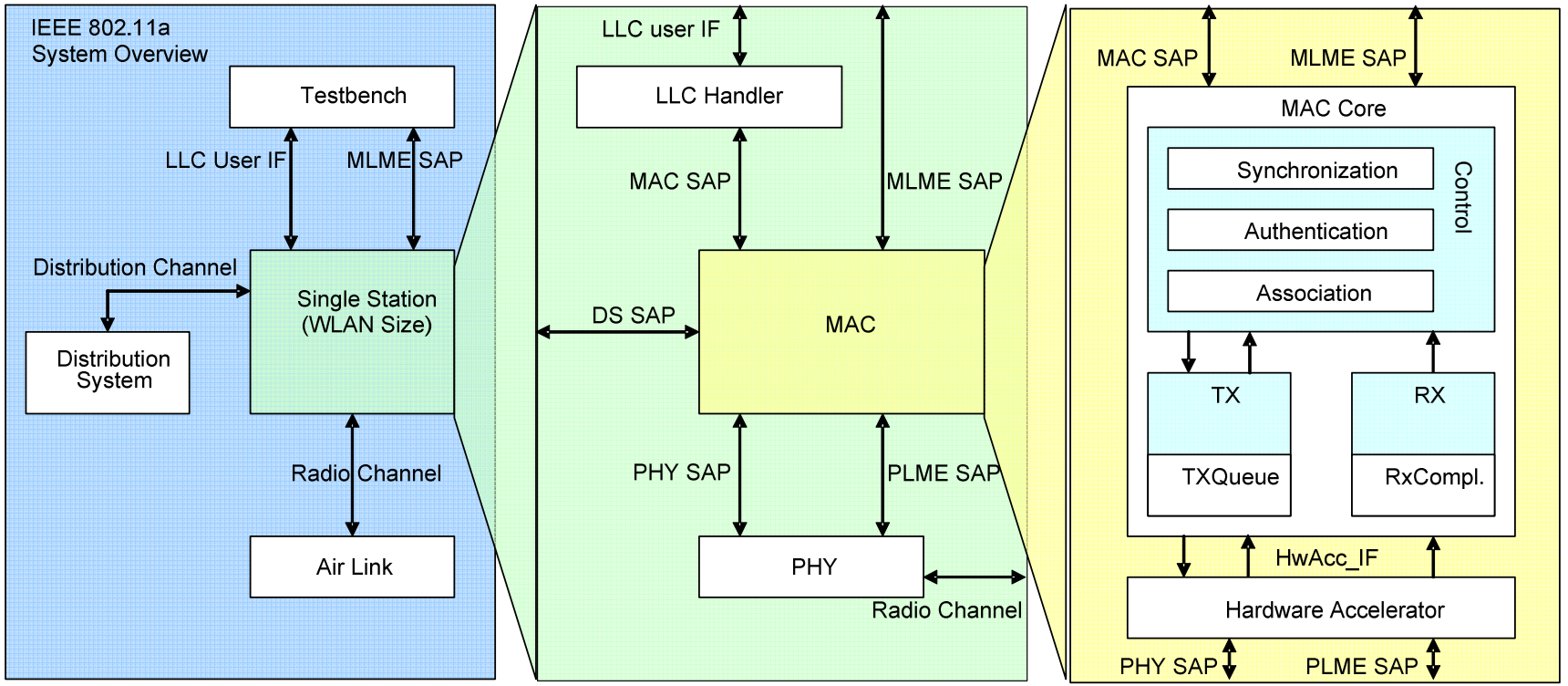
Area (mm^2)	9
Signal Ports	45
Power Ports	24
BIST Ports	5
Transistors ($x10^6$)	0.5
Memories (kbytes)	6
Power/Frequency (mW/MHz)	0.06
Maximum Frequency (MHz)	20

Design Flow of IEEE802.11a MAC SOC



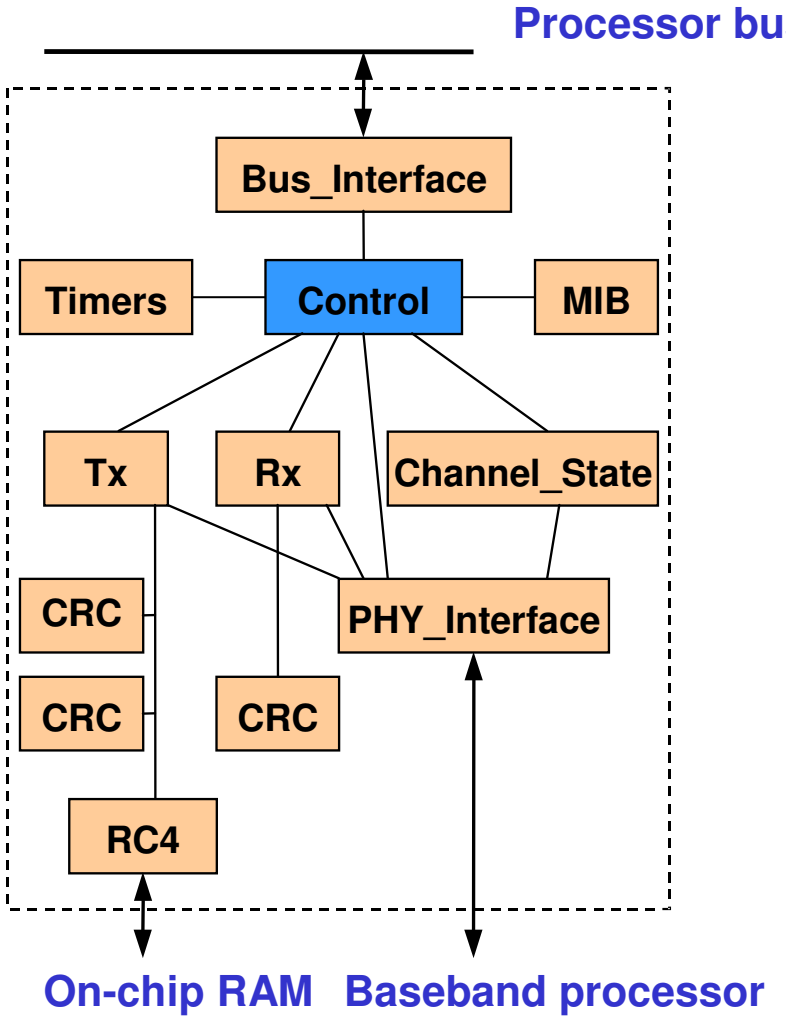
MAC Protocol Implementation

SDL Model



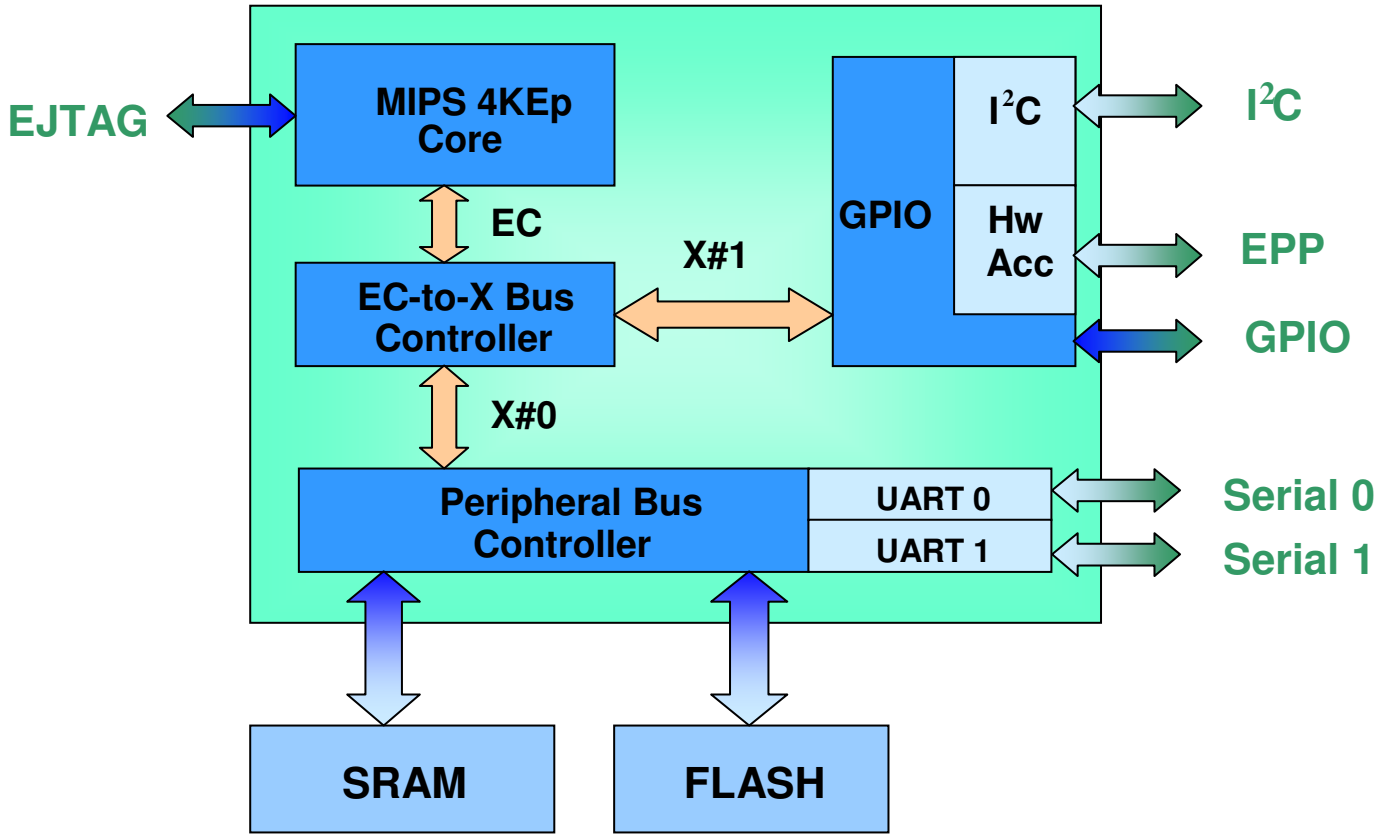
- Abstract protocol model
- Generation of C model
- Performance estimation in order to perform Hw/Sw partitioning

Hardware Accelerator



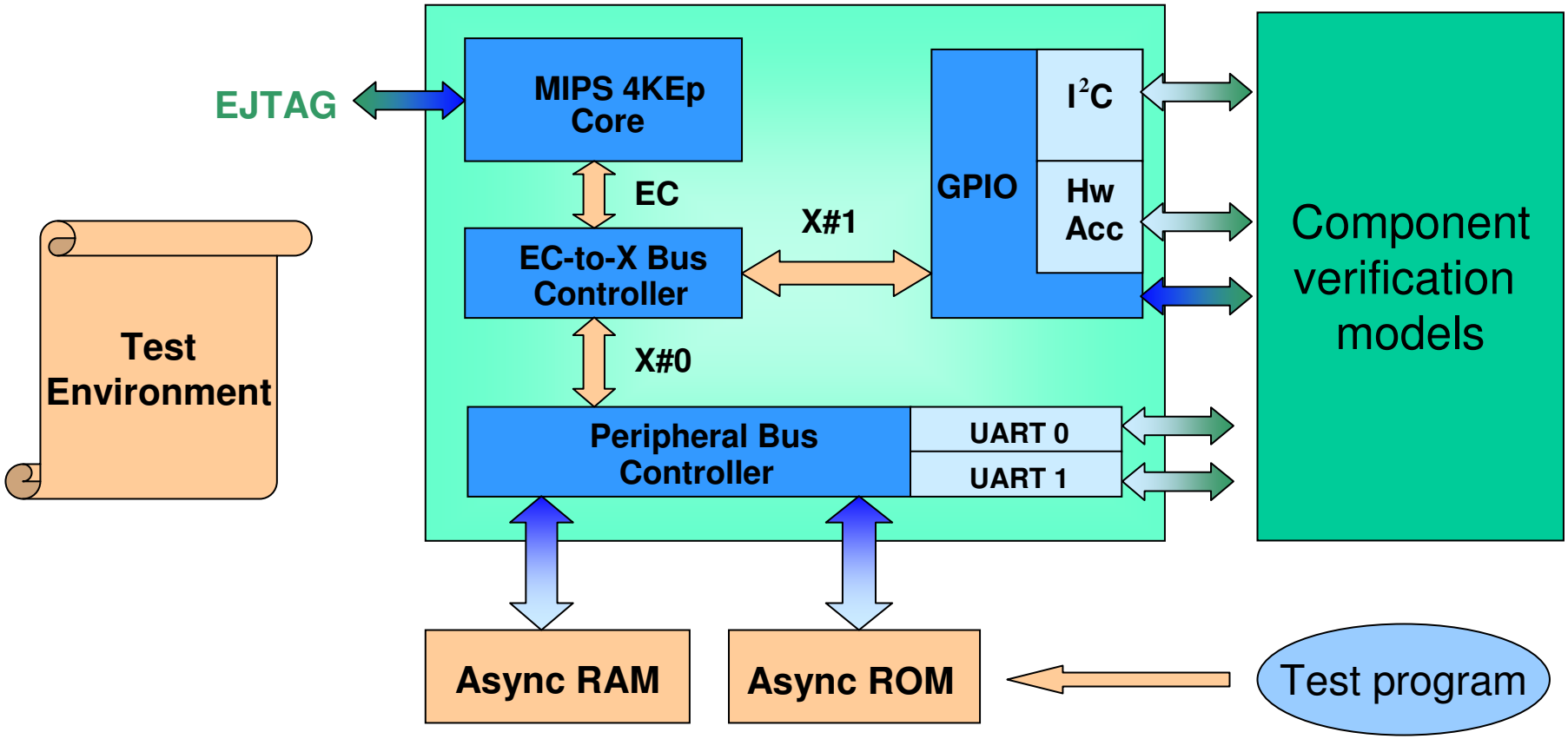
- executes timing critical MAC functions
  - Timers, CRC, RC4, address filter
- reduction of power consumption
- interface between baseband and CPU
- completely modeled in VHDL
- synthesized and simulated for 80MHz
- 5x512B single-port memory
- 2x256B dual-port memory
- soft resetable

System Architecture and Components



- Complete RTL description in VHDL/Verilog
- Synthesis scripts

Verification by Simulation

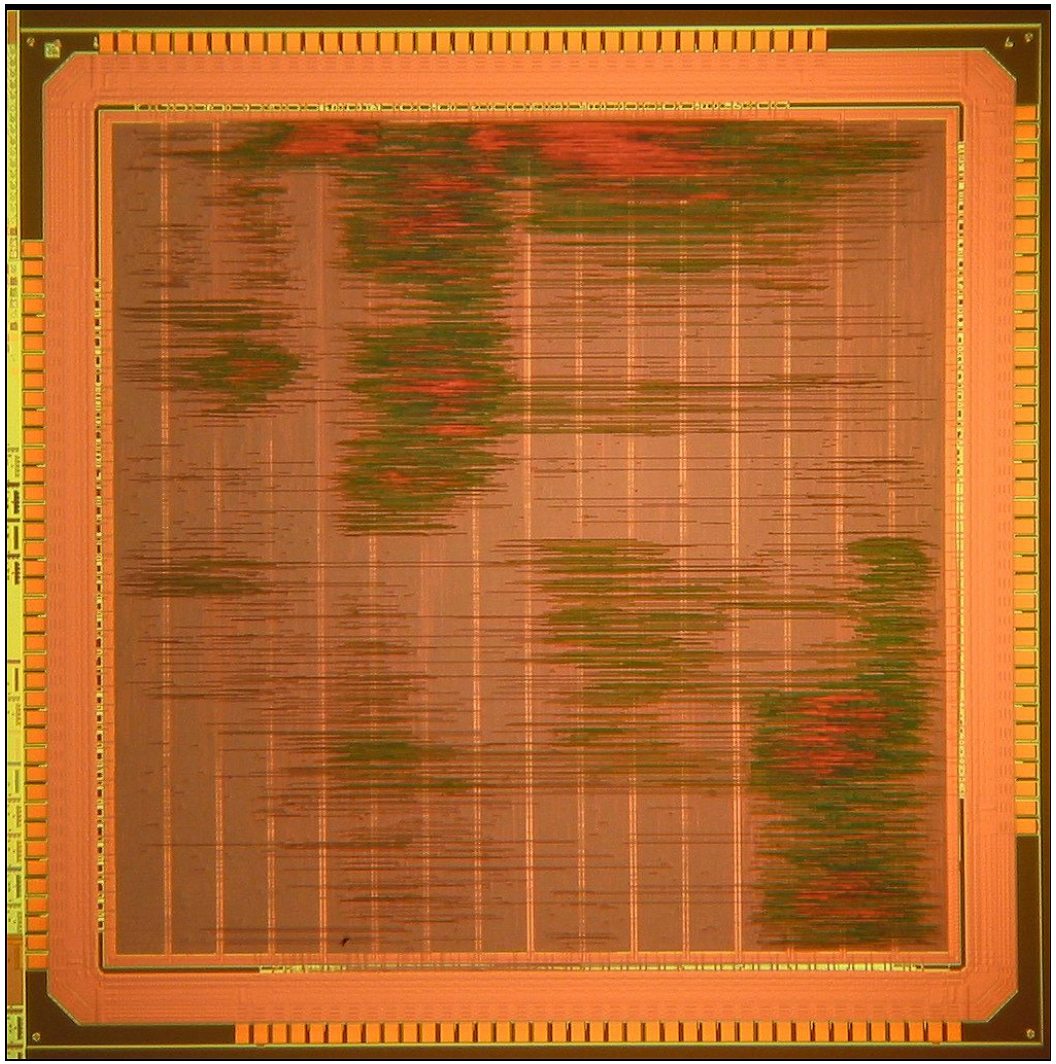


- Testbenches and simulation scripts

Synthesis Results

Design name	Estimated area (%)	Estimated power (%)
MIPS core	16.7	17
I ^{2}C bus controller	0.3	0.4
UART x 2	2.7	3.5
EC-to-X bus controller	3.4	0.8
Peripheral bus controller	0.8	1.6
Accelerator core	14.1	15.9
Single-port RAM 512B x 5	41.6	49.7
Dual-port RAM 256B x 2	19.4	9.5
GPIO	0.8	1.3
Glue logic	0.2	0.3
Chip	100	100

MAC SOC Layout



Technology: IHP 0.25µm CMOS

Area: ~ 30 mm2

Number of gates: 420,000 NAND

Number of pins: 140 signal + 16 power

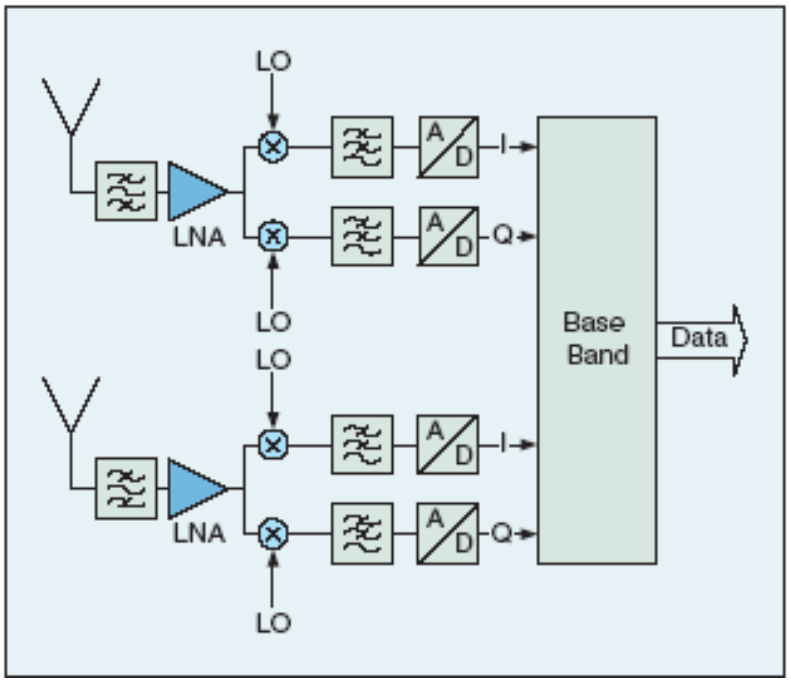
Package: PQFP 208L 28*28*3.35P0.5

Peak power: ~1W at 80 MHz, 2.5V

Chip testing: Agilent 93000

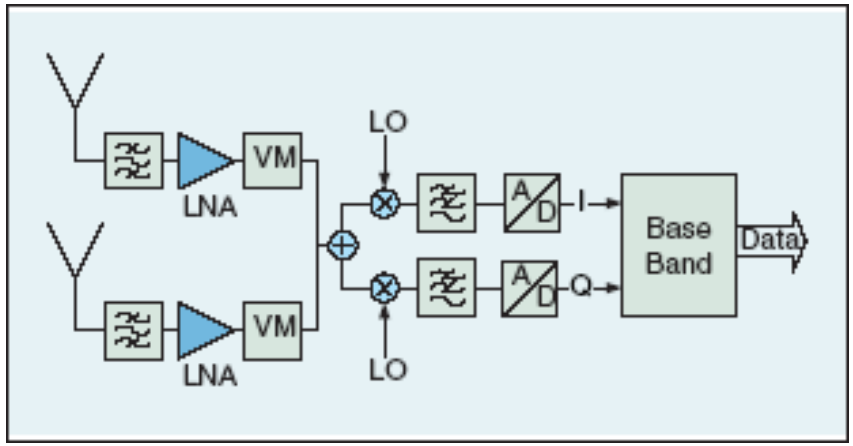
MIMO WLAN Transceivers

Traditional MIMO: Signal processing performed in the digital baseband



RF-MIMO: Signal processing performed in the analogue RF domain

Number of the digital basebands reduced to a single one



RF-MIMO (MIMAX) Transmitter and Receiver

Hardware overhead consists only of additional antennas and a modified RF front-end compared to a SISO system