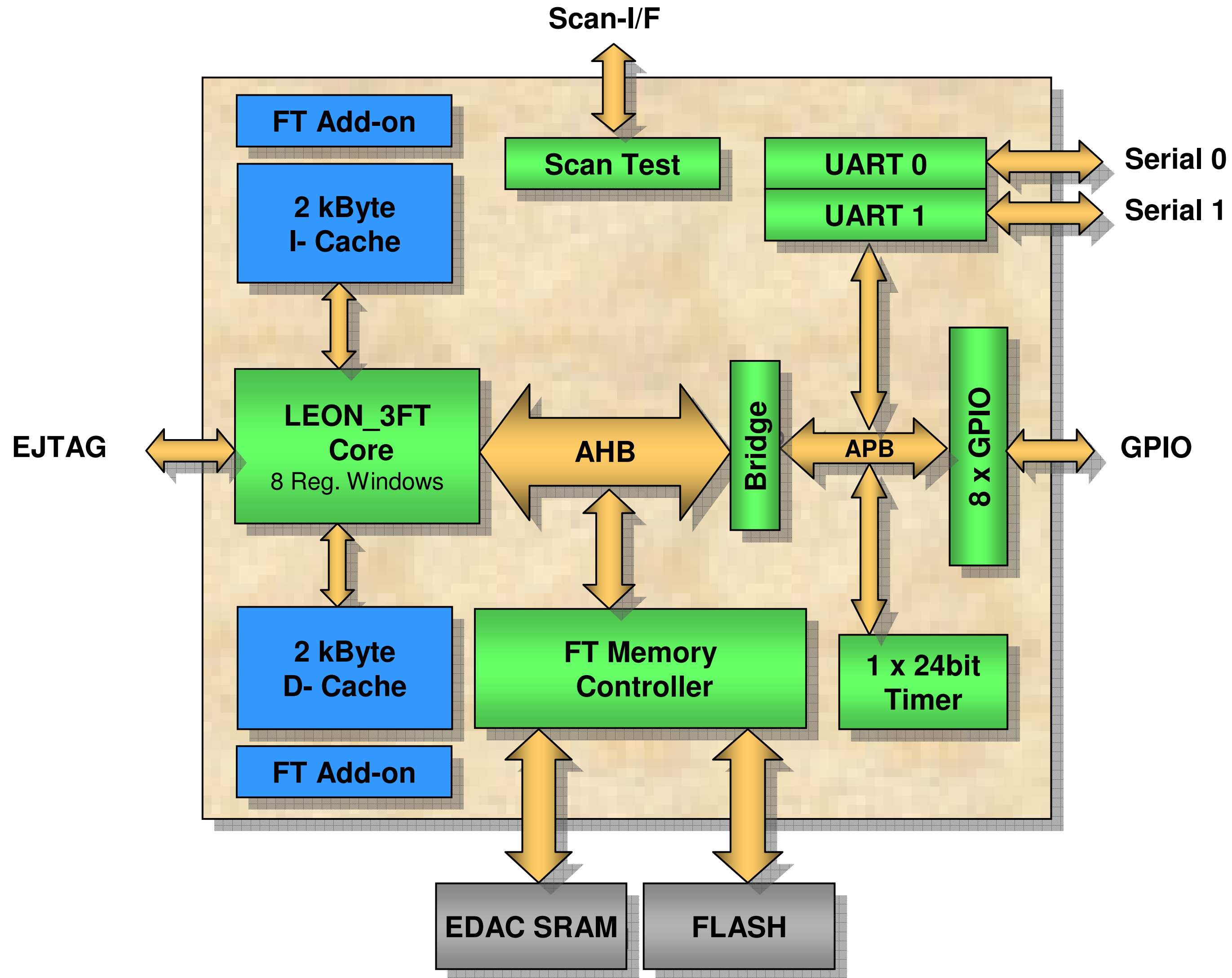
LEON3-FT Processor System

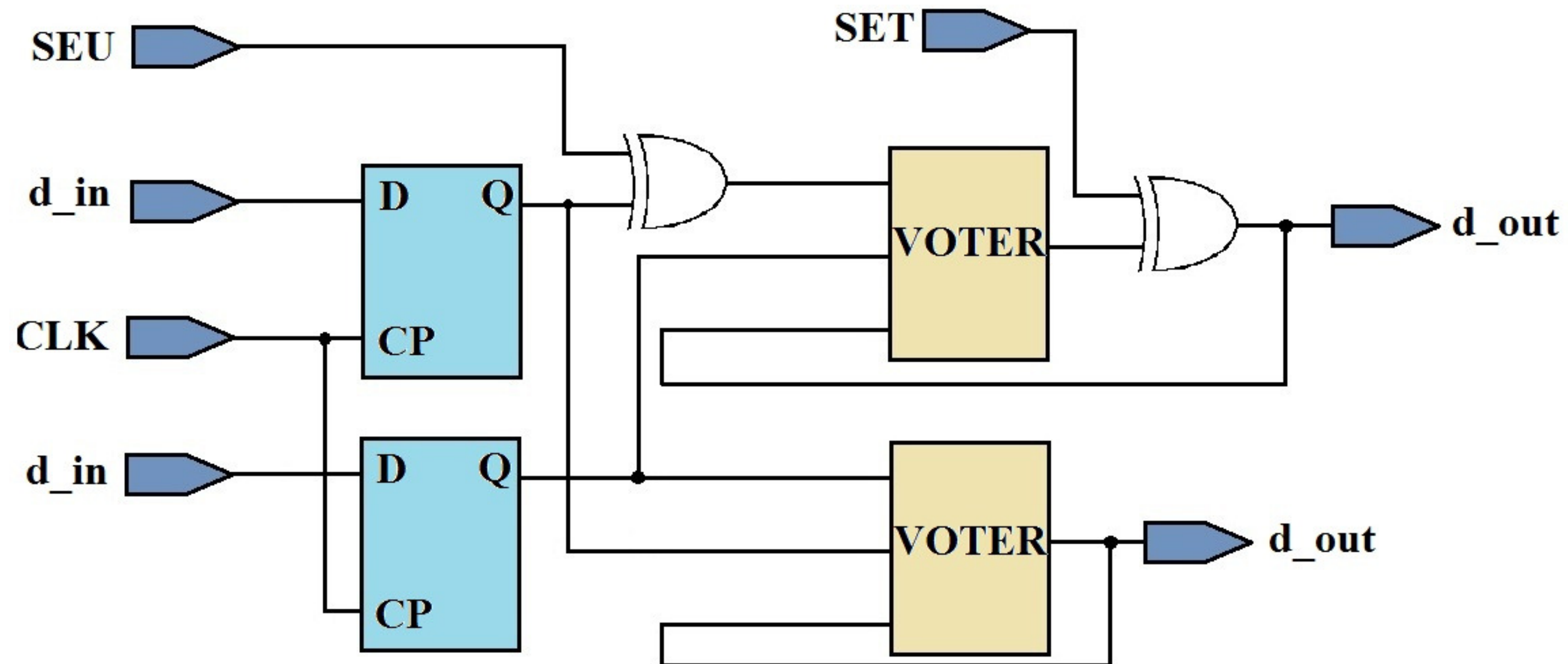


Implementation Details

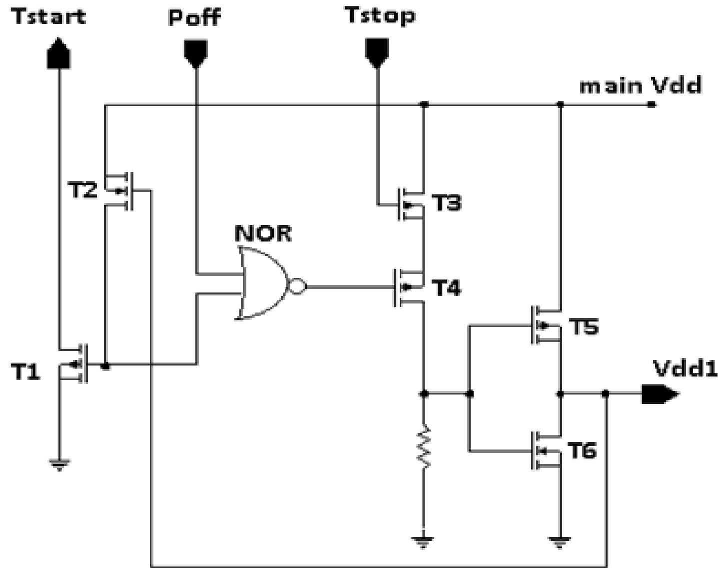
- **Installation of the release**
- **Adaptation of the configuration tool (to include IHP's library)**
- **Implementation of data and instruction caches**
- **Logic synthesis of the design**
- **Implementation of scan chain**
- **Generation of the chip layout**
- **Simulation (functional, post-synthesis and post-layout net-list)**
- **Scan test vectors generation (ATPG)**
- **Scan test simulation**
- **Adaptation of testbenches**
- **EVCD test vectors generation**
- **Test specification**
- **Documentation**

Double Modular Redundancy

- **Double Modular Redundancy with self-voting has 20% lower failure-free probability, 37% lower power consumption and 16% lower silicon area overhead than Triple Modular Redundancy**

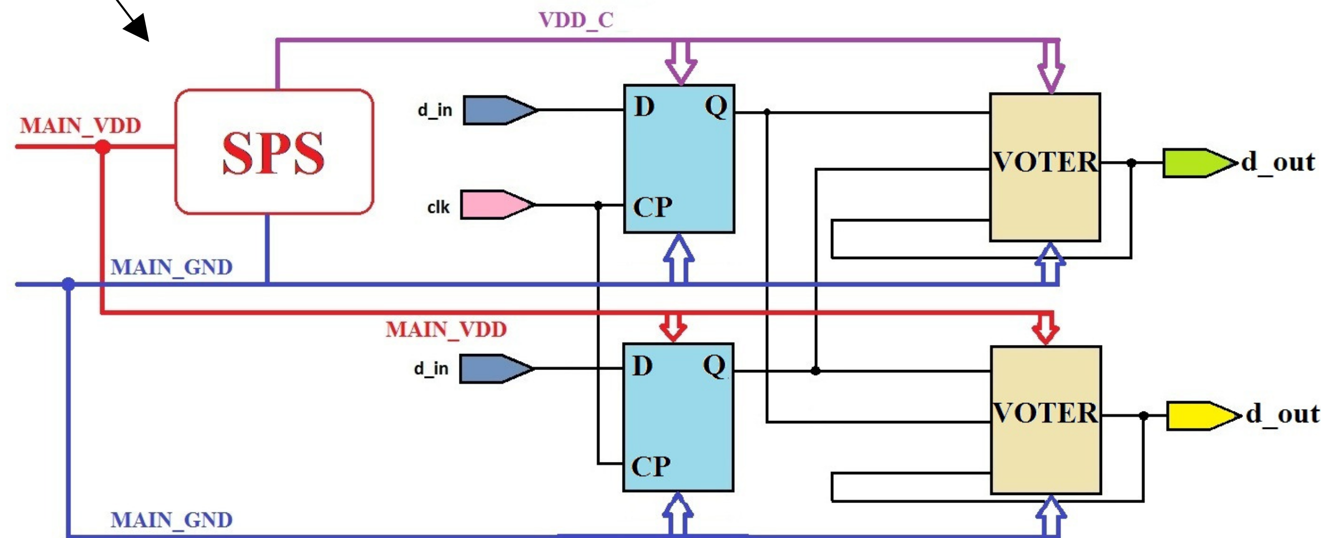


Protection Against Single Event Latchup

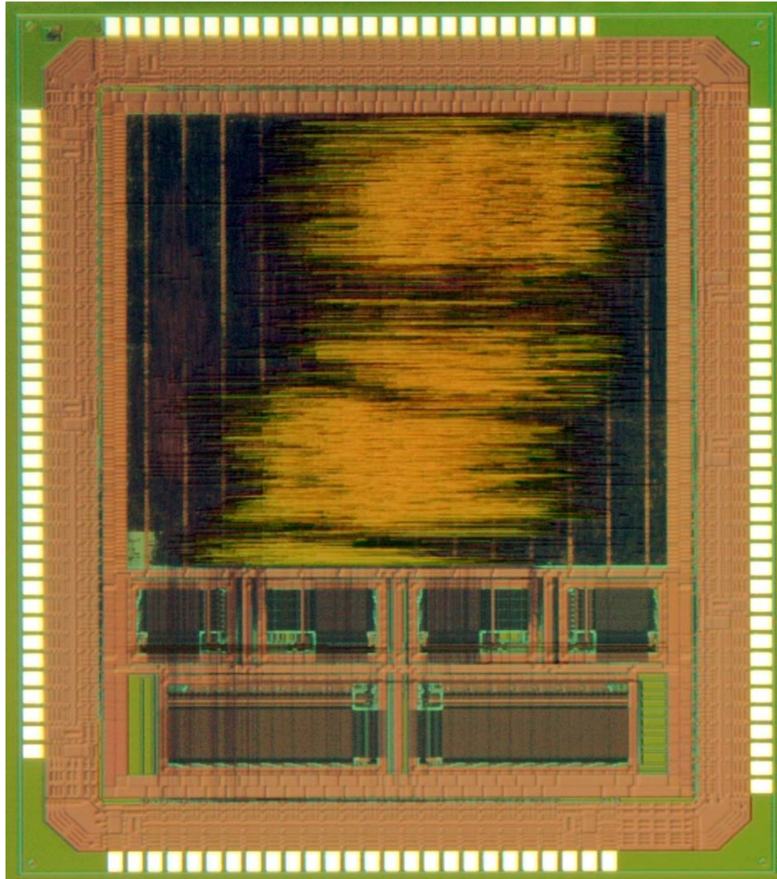


- Single event latchup effect requires design of a special power switch (SPS) cell
- Memories, EDACs and logic must be duplicated
- SPSs are placed under the cross-over points of the power stripes and standard cells
- SPS network is connected to the rest of power network in the power routing phase

- If VDD_C is short-circuited, T5 conducts high current
- Feedback line from Vdd1 = VDD_C causes T2 to switch on when this voltage is above the threshold voltage
- Automatically, T1 triggers Tstart output



Chip Features



LEON-3	
Area (mm^2)	22
Number of signal ports	105
Number of power ports	20
Number of scan ports	1 (3)
Transistors ($x10^6$)	0.83
Cache Memory (kB)	6
Scanable Flip-Flops ($x10^3$)	15
Power/Frequency (mW/MHz)	6.2
Max Frequency (MHz)	160

Cache Array	Size (KB)	No. of Words	Data Width	Address Width
I/D Data	2.5	512	36 of 40	9
I/D Tag	0.5	128	29 of 32	7

SOC Design-for-Testability

- **What is Scan-through-TAP?**

  Use of IEEE Standard 1149.1 user instruction to concatenate the internal scan chain with the BSR chain to perform a single chain operation

- **What do we achieve implementing Scan-through-TAP?**

  Reduction of the scan pins number

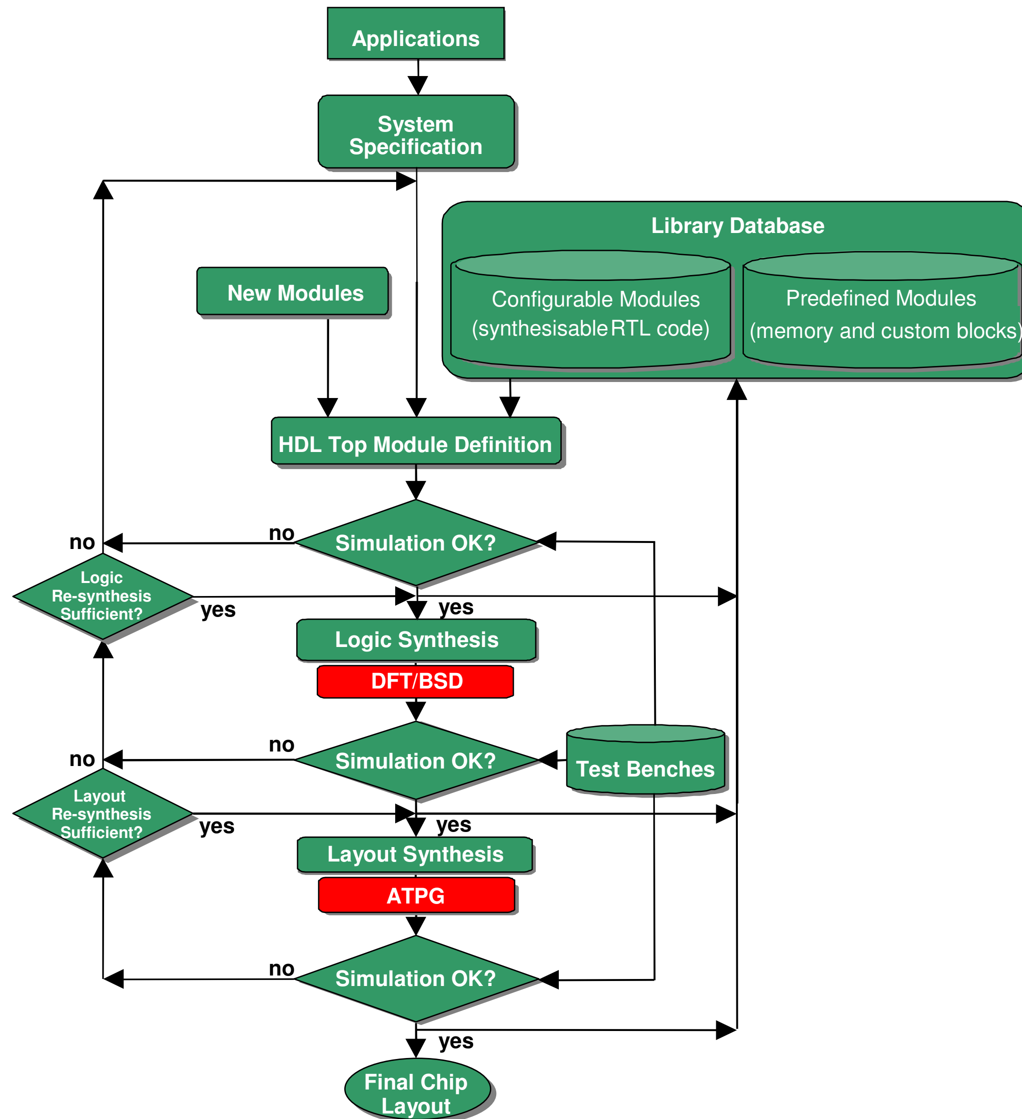
  Accessibility of the internal scan chains through the TAP controller

  Single shift path through for burn-in and diagnostics

- **What kind of EDA tools do we need?**

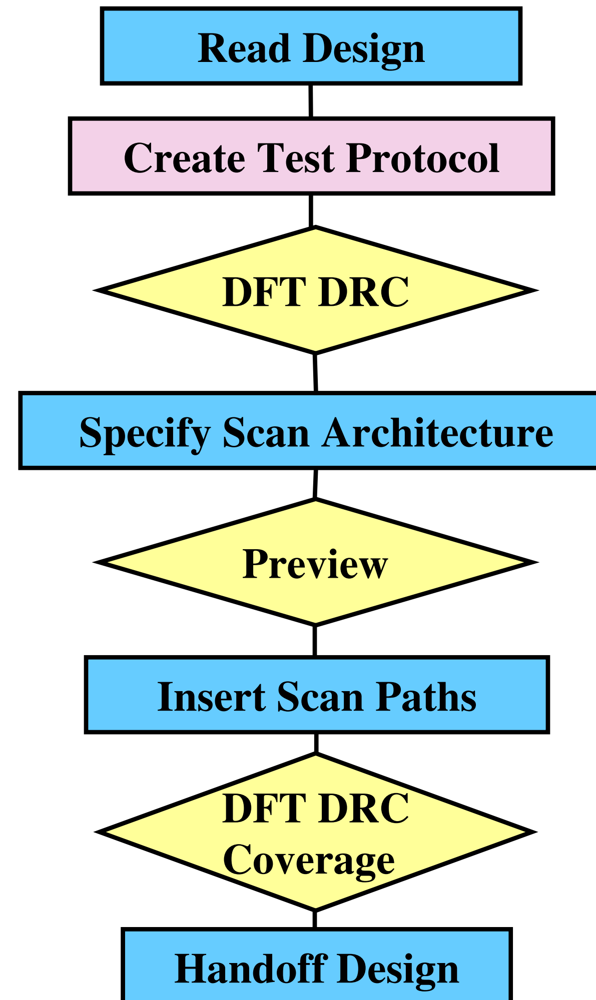
  Standard synthesis, DFT, BSD, and ATPG tools

DFT/BSD in SOC Design Flow

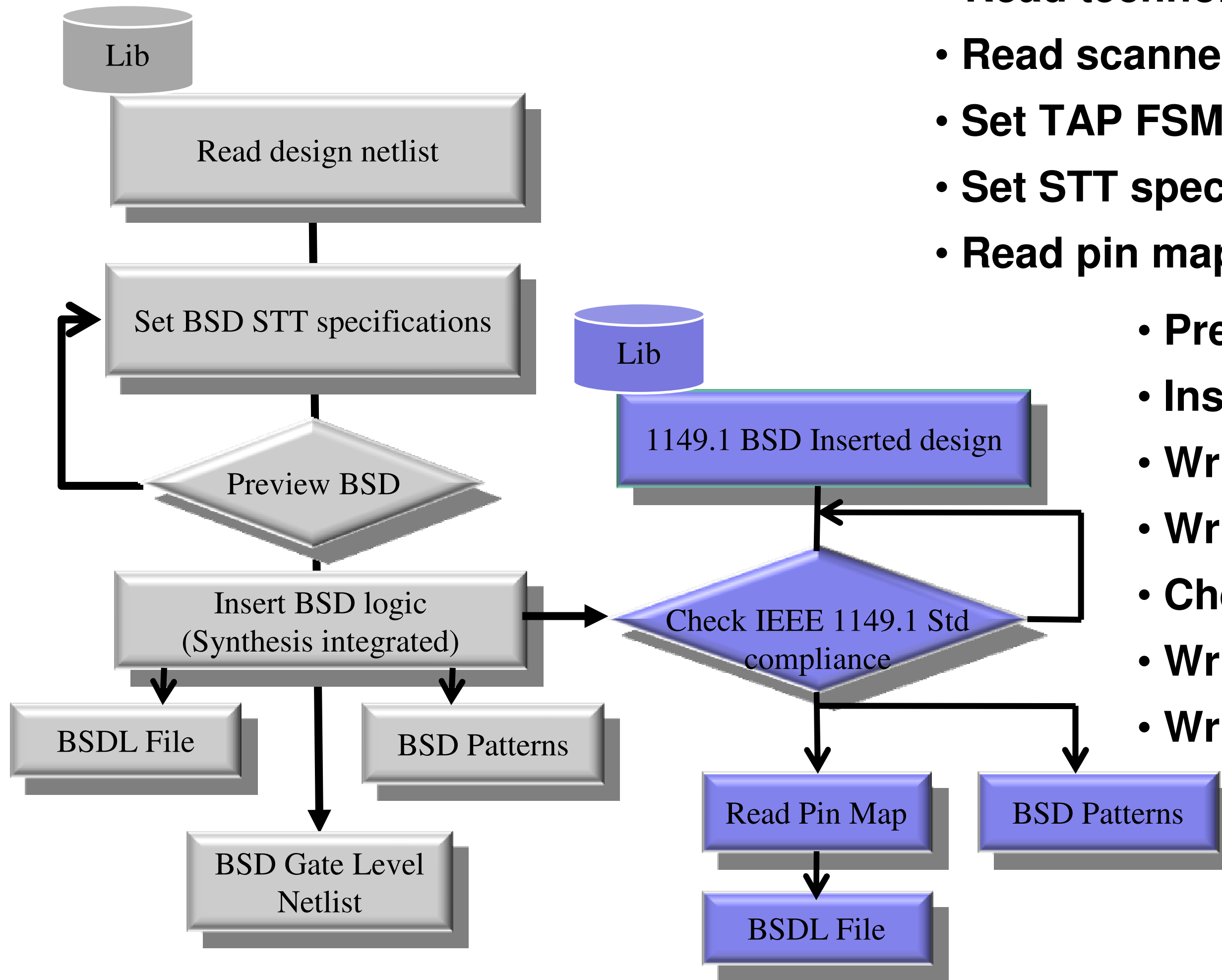


Scan Insertion Flow

- Read in synthesized design
- Define clock constraints
- Define scan chain
- Insert scan chains
- Write out scan test protocol and netlist for TetraMAX

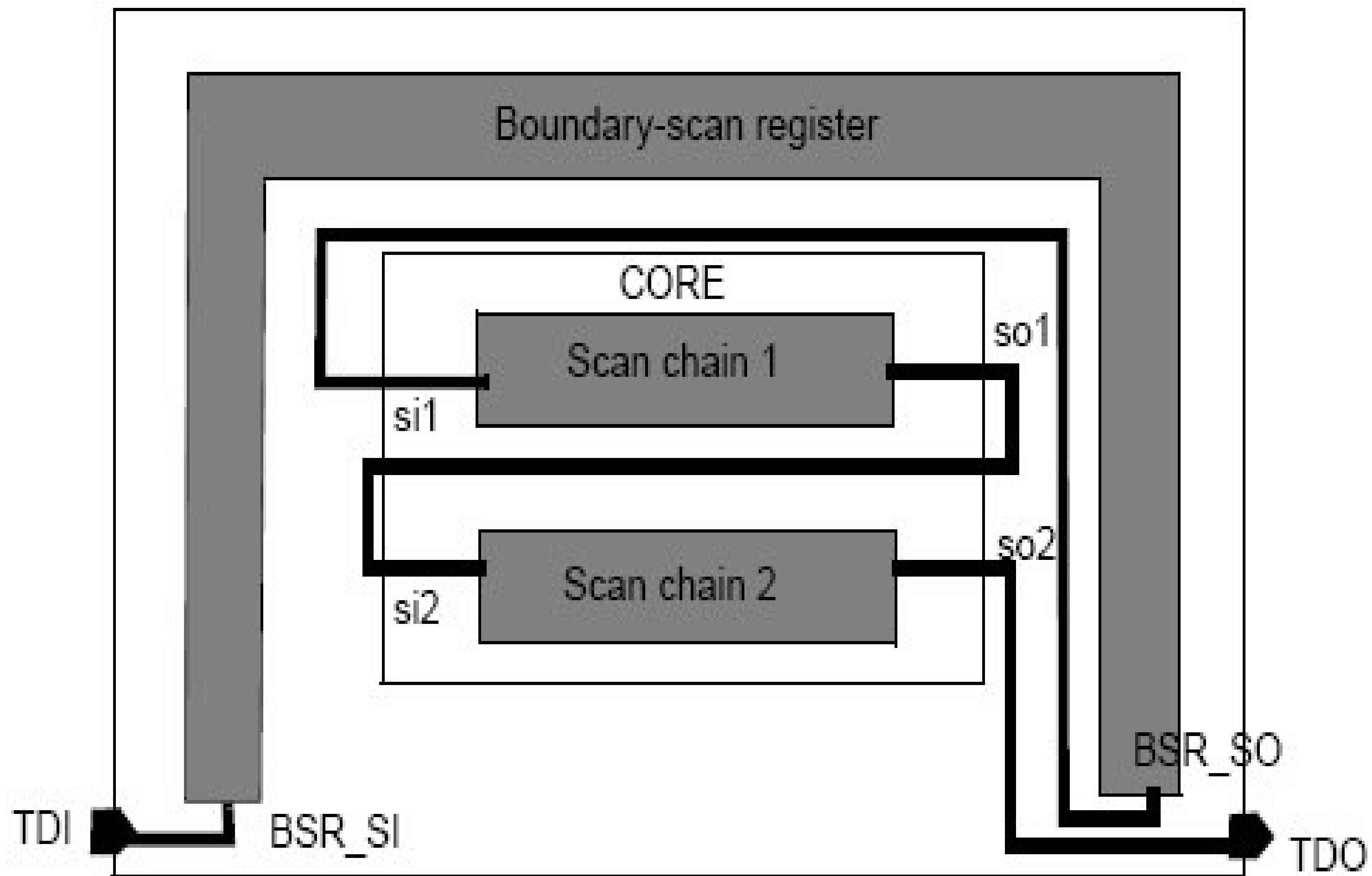


Boundary Scan Insertion Flow

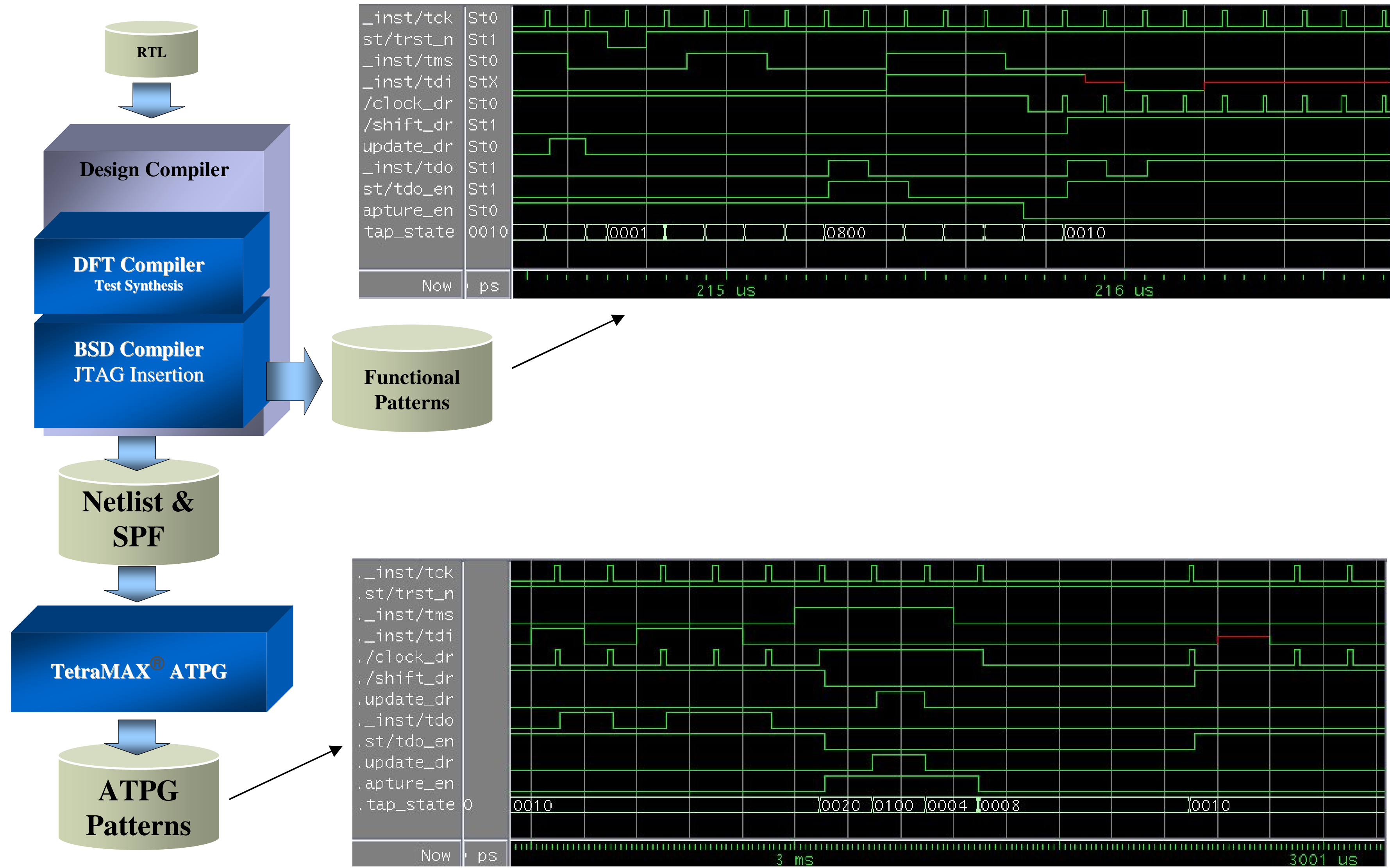


- **Read technology synthesis libraries**
- **Read scanned ready netlist with IOs**
- **Set TAP FSM specification**
- **Set STT specification**
- **Read pin map for die package BSR order**
- **Preview your JTAG design**
- **Insert your JTAG logic**
- **Write out final netlist**
- **Write BSDL file and patterns (optional)**
- **Check compliance to IEEE 1149.1 STD**
- **Write BSDL file and BSD patterns**
- **Write the STIL protocol file for ATPG**

Scan-Through-TAP Register



STT Test Patterns



Implementation Results

- Single scan register made of around 15000 scan flip-flops
- Boundary scan register of 151 cell
- 5 TAP instructions
  - BYPASS
  - EXTEST
  - PRELOAD
  - SAMPLE
  - STT
- 32000 BSD functional test patterns
- 1151 ATPG test patterns
- Chip area overhead below 7%
  - Caused by insertion of scan flip-flops and boundary scan logic
- Combined fault coverage is slightly above 94%

Links for More Information

- http://www.tandem-projekt.de
- http://www.ict-mimax.eu
- http://www.mips.com
- http://www.gaisler.com
- http://www.arm.com
- http://www.tensilica.com